Device description

The IQ-9075 (also known as the QCS9075) is part of the IQ9 Series Platform SoCs, offering unparalleled on-device AI performance for the most demanding industrial applications. It provides design flexibility for high-compute, power-efficient performance, capable of handling heavy workloads in extreme environments.

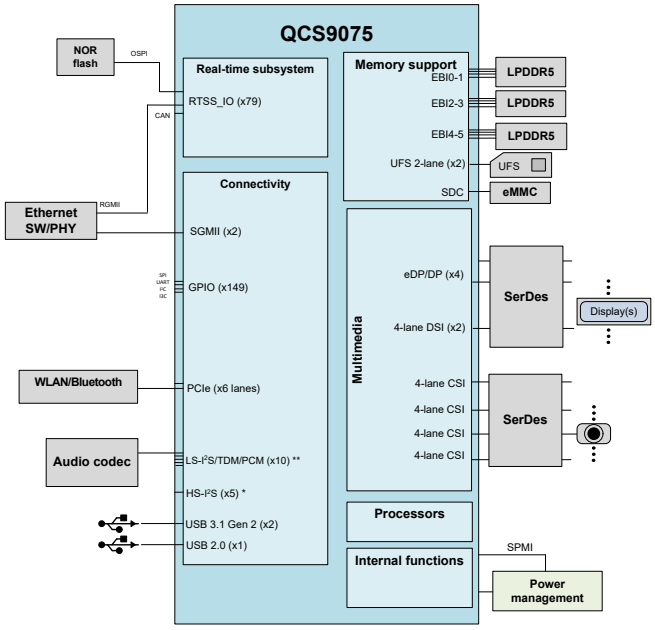
The QCS9075 device features the following major architectural blocks:

- Qualcomm® Kryo™ Gen 6 CPU built on Arm v8.2 Cortex technology
- Qualcomm® Adreno™ 663 GPU for the highest in graphics performance and power efficiency
- Qualcomm® Hexagon™ Tensor Processor integrated with Qualcomm Hexagon DSP, quad Qualcomm Hexagon Vector eXtensions (HVX) processor, and dual Qualcomm Hexagon Matrix eXtensions (HMX) coprocessors for high performance machine learning use cases.

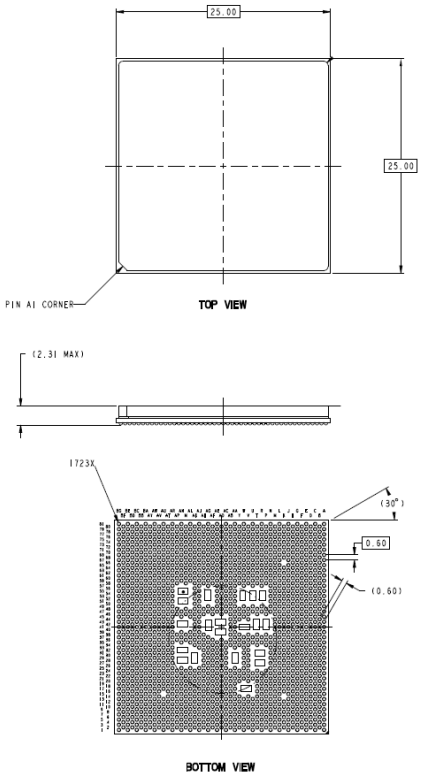
Key features

- Qualcomm Spectra™ ISP 690 image processing engine
- Advanced camera: 4 × 4-lane CSI ports with 16+ concurrent cameras (requires off-chip MIPI-aggregation) support to allow for flexibility for industrial deployments.
- Qualcomm Adreno™ 765 VPU for high-quality, ultra HD video encode and decode
- Dual Adreno DPU 1199 for ultra HD multi-display support
- Advanced AI performance: Up to 100 TOPS supporting a broad set of AI models with AI Hub using a mature toolset for advanced AI functions.
- Expanded temperature range: Junction temperature range from -40°C to 115°C suitable for most demanding industrial usages and environments.
- Dedicated real-time subsystem (RTSS) equipped with quad Cortex-R52 CPU configurable per pair in lock-step mode or split-mode.
- Real-time subsystem: Cortex R52 based independent RTSS (MCU like) having 1GbE ethernet with time sensitive network (TSN), and CAN-FD.
- Robust I/O: Increased PCIe, USB capabilities supporting a wide variety of peripherals; integrated ethernet (with TSN) for wired connectivity.

QCS9075 high-level block diagram and FCBGA1723+HS package outline drawing



* 2 of the 5 HS-I²S interfaces are muxed behind I²S interfaces
** 10 LS I²S interfaces include 7 dedicated LS I²S and 3 dedicated HS I²S reconfigured as LS I²S interfaces.



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1 Introduction

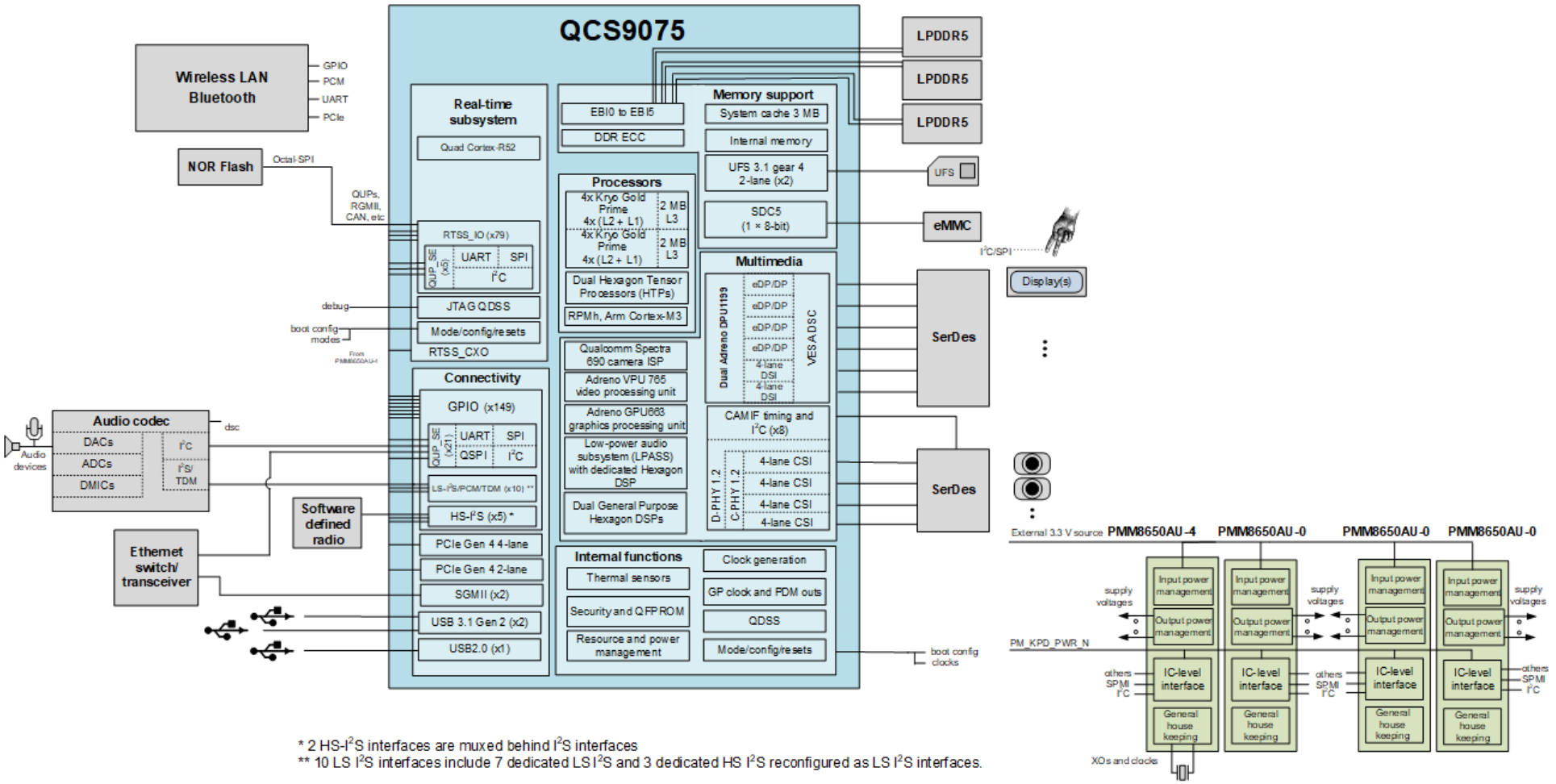
Document updates

See the Revision history for details on the changes included in this revision.

NOTE All the information provided is preliminary and is subject to change before CS.

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1.1 Functional block diagram



* 2 HS-I²S interfaces are muxed behind I²S interfaces
** 10 LS I²S interfaces include 7 dedicated LS I²S and 3 dedicated HS I²S reconfigured as LS I²S interfaces.

Figure 1-1 QCS9075 functional block diagram

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1.2 QCS9075 features

NOTE Some of the hardware features integrated within the QCS9075 must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled QCS9075 features.

Table 1-1 QCS9075 features

Feature	QCS9075 capability
Processors	
Applications	Kryo Gen 6 CPU subsystem - two identical quad-core cluster with full hardware coherency in between ■ Quad Kryo Gold Prime cores with 512 kB L2 cache per core at 2.361 GHz (optional support to go up to 2.55 GHz) ■ 2 MB shared L3 cache per cluster
Digital signal processing	Dual Hexagon Tensor Processor integrated with Qualcomm Hexagon DSP, up to 1.420 GHz, quad Hexagon Vector eXtensions (HVX), and dual Hexagon Matrix eXtensions (HMX) co-processors ■ Common AI processing architecture for machine learning use cases ■ Matrix co-processors (one HMX-Integer and one HMX-float per Hexagon Tensor Processor) for deep neural network acceleration Audio Hexagon DSP dedicated to audio subsystem, up to 1.344 GHz and with a 2 MB L2/TCM Two general purpose Hexagon DSPs up to 1.708 GHz and with a 1 MB L2 cache for advanced audio processing and other use cases All Hexagon DSPs are cache-based processors with full access to DDR memory
Artificial intelligence (AI)	Up to 100 dense/200 sparse INT8 TOPS Llama 2 7B: 22 tokens per second
Real-time subsystem (RTSS)	■ A subsystem integrated with quad cortex-R52 CPU ■ Each cortex-R52 CPU frequency is up to 1.850 GHz ■ Independent booting capability through OSPI interface
Always-on subsystem	■ Always-on subsystem with always-on processor ■ Hardware-based resource and power management (RPMh) with hardware accelerators for voltage control and regulation, clock management, and resource communication
Memory support	
System memory via EBI	■ Six-channel high-speed memory – 3200 MHz LPDDR5 SDRAM (6 × 16-bit) ■ 3 MB system cache
Other internal memory	■ 256 kB IMEM ■ 1.5 MB GMEM for graphics ■ 1 MB L2 cache and 8 MB Vector-TCM (vTCM) for each Hexagon Tensor Processor
External memory	
Via UFS	Two UFS 3.1 gear 4 – two lanes for on-board memory (UFS0 as main domain boot up device)
Via eMMC	1 × 8-bit SDIO interface (SDC1) to support eMMC 5.1. [a]

Table 1-1 QCS9075 features (cont.)

Feature	QCS9075 capability
Via Octal/Quad SPI	NOR flash memory running up to 166 MHz as RTSS domain boot up device
Via PCIe	NVMe (non-bootable)
Multimedia	
Adreno display processing unit (DPU) Display interface/performance	Dual Adreno DPU1199 Two 4-lane MIPI DSI with VESA DSC v1.2 ■ D-PHY v1.2: 2.5 Gbps/lane on four lanes per port, 10 Gbps/port, up to 20 Gbps total ■ C-PHY v1.1: 5.7 Gbps/trio on three trios per port, 17 Gbps/port, up to 34 Gbps total Four Embedded DisplayPorts (eDP)/DisplayPort (DP) v1.4 at 8.1 Gbps/lane, 32.4 Gbps/port, MST and VESA DSC v1.2a and forward error correction (FEC) ■ Up to a maximum of 48 MP; example configuration: 5 × 4K
Image processing	Destination scaler, fetch exclusion rect., inline rotation, 17 × 17 × 17 3D LUT (ViG/DSPP), HDR10 improvements WCG, Rounded-corner, CCCS to Fixed-point
Compression	UBWC 4.0, DSC v1.2
Camera support	
Performance	Qualcomm Spectra 690 ISP ■ Pixel processing: 2 × IFE + 5 × IFE_L ■ Data format inputs: 24 bit HDR RGGB/RCCB/RYYCy, RCCG, YUV ■ Data format outputs: 12/10/8 bit Y, 10/8 bit UV; RGB8 in planar or interleaved order
Camera interface	Processing features: 24b HDR Bayer processing, lens distortion correction, advanced tone mapping, offset correction, lens roll off correction, bad pixel correction, directional scalers, color LUTs, color space transform, noise reduction Four MIPI CSI interfaces configurable as D-PHY or C-PHY mode ■ D-PHY v1.2: 2.5 Gbps/lane on four lanes per port, 10 Gbps/port, up to 40 Gbps total. Each 4-lane port can also be configured as 1-lane + 2-lane ports or 1-lane + 1-lane ports ■ C-PHY v1.2: 10.2 Gbps/trio on three trios per port, 31 Gbps/port, up to 123 Gbps total. Each 3-trio port can also be configured as 1-trio + 2-trio ports, or three 1-trio ports
Adreno video processing unit (VPU)	■ Adreno VPU 765 – fifth-generation UHD video processing unit ■ Video decode up to UHD275 ■ Video encode up to UHD170 ■ Concurrent UHD120 decode + UHD60 encode or UHD60 decode + UHD120 encode ■ Native decode support for AV1, HEVC, H.264, H.265, VP9, MPEG-2 codecs ■ Native encode support for HEVC, H.264 and H.265 ■ Embedded video analytics (EVA) for optical flow processing and stereo disparity
Adreno graphic processing unit (GPU)	■ Adreno 663 GPU supports safe GPGPU compute, up to 840 MHz ■ Graphics APIs: Vulkan 1.2, OpenGL ES 3.2 ■ Compute APIs: Vulkan 1.2, OpenCL 2.0 FP, Adreno NN Direct

Table 1-1 QCS9075 features (cont.)

Feature	QCS9075 capability
Low-power audio subsystem (LPASS)	■ Dedicated audio LPASS Hexagon DSP with a 2 MB L2/TCM ■ AI Processor (eNPU) to accelerate neural networking use cases ■ HW linear echo cancellation accelerator ■ Two general purpose DSPs to offload audio high performance use cases
Audio interfaces	
LS-I^{2}S (muxed with PCM/TDM pins)	■ Up to 10 (7 + 3) interfaces (pin multiplexed with PCM/TDM interfaces): nine (6 + 3) interfaces with two data lanes each; one interface with four data lanes for a total of 22 (16 + 6) data lanes ■ Three MCLKs up to 512 × 48 kHz (24.576 MHz); clock master or slave independent of the source of frame sync/word select ■ Supports two channels of 32-bit sample up to 384 kHz sample rate, for each data line
PCM/TDM (muxed with LS-I^{2}S and HS-I^{2}S pins)	■ Multi-lane TDM (master and slave capable) ■ Up to 10 (7 + 3) interfaces (pin multiplexed with I^{2}S): nine (6 + 3) interfaces with two data lanes each; one interface with four data lanes ■ Short, long, and one-slot sync mode ■ Maximum clock frequency of 24.576 MHz (muxed with LS-I^{2}S) or 73.728 MHz (RX, muxed with HS-I^{2}S) □ Up to 512 bits/frame, 32 bits/slot, 16 slots/interface with 48 KHz sample rate ■ Support TDM interfaces grouping for data synchronization
HS-I^{2}S(muxed with PCM/TDM pins)	■ Five high-speed (up to 73.728 MHz) receive interfaces for software defined radio (SDR); two of them are muxed behind LS-I^{2}S interfaces; all of them can be configured as LS-I^{2}S interfaces if needed ■ Two receive-only data lanes per interface; clock and word select in slave mode **NOTE** The additional LS-I^{2}S interfaces (muxed with PCM/TDM pins) are configured from the three dedicated HS-I^{2}S interfaces.
Connectivity	
Qualcomm universal peripheral (QUP) serial engines	■ 21 main domain (MD) GPIO-based QUP SEs: 7 bits for QUP3_SE_0, 5 bits for QUP2_SE_2 and 4 bits for each of the other 19 QUP SEs; multiplexed serial interface functions ■ Five RTSS domain GPIO-based QUP SEs: 5 bits for QUP0_SE_4 and 4 bits for each of the other four QUP SEs; multiplexed serial interface functions
UART (up to 4 MHz)	UART (64 B FIFO) interface available on all MD and RTSS domain QUP SEs, except MD QUP0_SE_2/3, QUP1_SE_2/3, QUP2_SE_2/3 and RTSS QUP0_SE_2/3, which also support HS-UART (128 B FIFO)
I^{2}C master (up to 1 MHz)	I^{2}C interface available on MD and RTSS domain QUP SEs, dedicated controller for each port
SPI master (up to 50 MHz)	SPI master interfaces available on all MD and RTSS domains QUP SEs, except for MD QUP1_SE_6
SPI slave (up to 50 MHz)	SPI slave interface available on MD QUP0_SE_4/5, QUP1_SE_4/5, QUP2_SE_4/5 and RTSS QUP0_SE_0/1
QSPI (up to 100 MHz)	QSPI interface is available on QUP3_SE_0
CCI I^{2}C	Eight dedicated I^{2}C interfaces for devices using CSI ports

Table 1-1 QCS9075 features (cont.)

Feature	QCS9075 capability
USB	Three total USB interfaces ■ One USB 3.1 Gen 2 - USB0 (HS + SS, support device and host modes) ■ One USB 3.1 Gen 2 - USB1 (HS + SS, support device and host modes) ■ One USB2.0 - USB2 (HS, support device and host modes)
PCIe	■ One 2-lane PCIe Gen4: PCIe0 (RC + EP) ■ One 4-lane PCIe Gen4: PCIe1 (RC + EP)
RGMII	One RTSS domain RGMII interface with MDIO for ethernet with AVB
CAN-FD	Eight CAN-FD interfaces located in RTSS domain, each of them supports up to 10 Mbps
SGMII	Two SGMII interfaces supporting up to 2.5 Gbps each
Configurable GPIOs	
Number of main domain GPIO ports	149 – GPIO_0 to GPIO_148
Number of RTSS domain GPIO ports	79 – RTSS_IO_0 to RTSS_IO_78
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current up to 16 mA
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
Crypto	Hardware ECC and RSA (Elliptic-Curve Cryptography), ICE, Crypto engine v5 (CE5), FIPS/CAVP certifiable, RNG (random number generation)
QFPROM	Fuse bits available for OEM use
Access control	Programmable security domain protection and sand-boxing Content Protection Zone (CPZ) supported
Secure boot and tools	Secure Boot with Sec Tools 5.4; easy to use tool set
Storage security	Secure file system (SFS); fast trusted storage
TrustZone	Qualcomm® Trusted Execution Environment (QTEE v5.3)
QTEE services	KeyMaster and Gate Keeper, Widevine, Wired HDCP2.x, SHE emulation in TEE
ICEMEM	An inline encryption/decryption engine used to protect the confidentiality of external RAM
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Dedicated 19.2 MHz RTSS_CXO for RTSS ■ 19.2 MHz CXO_0 and CXO_1 as clock sources for main domain of the chip ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG
Others	Thermal sensors; modes and resets; peripheral subsystem
Chipset interface features	
Power management	Two-line SPMI; plus other lines, as needed via GPIOs

Table 1-1 QCS9075 features (cont.)

Feature	QCS9075 capability
Fabrication technology and package	
Package type and dimensions	FCBGA1723+HS: 25.0 x 25.0 x 2.31 mm; maximum (including metallic heat spreader)

[a] 2 × UFS and 1 × eMMC cannot be supported together. More details on the eMMC support will be added in a future revision of this document.

2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O description (pin type) parameters

Symbol	Description
Pad type	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (Hi-Z) output
Padpull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
PX_0	Pad group 0 for main domain (control signals); 1.8 V
PX_0_BPP	Pad group 0 _BPP (back power protection); 1.8 V
PX_1	Pad group 1 (EBI I/O); 1.1 V
RTSS_PX_0	Pad group 0 for RTSS domain (control signals); 1.8 V
PX_3	Pad group 3 (most peripherals); 1.8 V
PX_3_BPP	Pad group 3_BPP (back power protection I/Os); 1.8 V
PX_7	Pad group 7 (SDC1- eMMC); 1.8 V
RTSS_PX_3	Pad group 3 for RTSS domain (most peripherals); 1.8 V
RTSS_PX_3_BPP	Pad group 3_BPP (back power protection I/Os) for RTSS; 1.8 V

Table 2-1 I/O description (pin type) parameters (cont.)

Symbol	Description
RTSS_PX_8	Pad group 8 for RTSS domain (RGMII_0); 1.8 V or 2.5 V
PX_9	Pad group 9 (UFS0_REF_CLK and UFS0_RESET); 1.2 V
PX_10	Pad group 10 (UFS1_REF_CLK and UFS1_RESET); 1.2 V
PX_11	Pad group 11 (CXO); 1.8 V
RTSS_PX_11	Pad group 11 for RTSS domain (CXO); 1.8 V

2.2 Pin map

The QCS9075 chipset is available in the FCBGA1723+HS that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details. A high-level view of the pin assignments is shown in the following figure.

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QCS9075 + PMM8650AU Pin Assignment and GPIO Configuration Spreadsheet (80-73417-1A) lists all QCS6490 and QCS5430 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

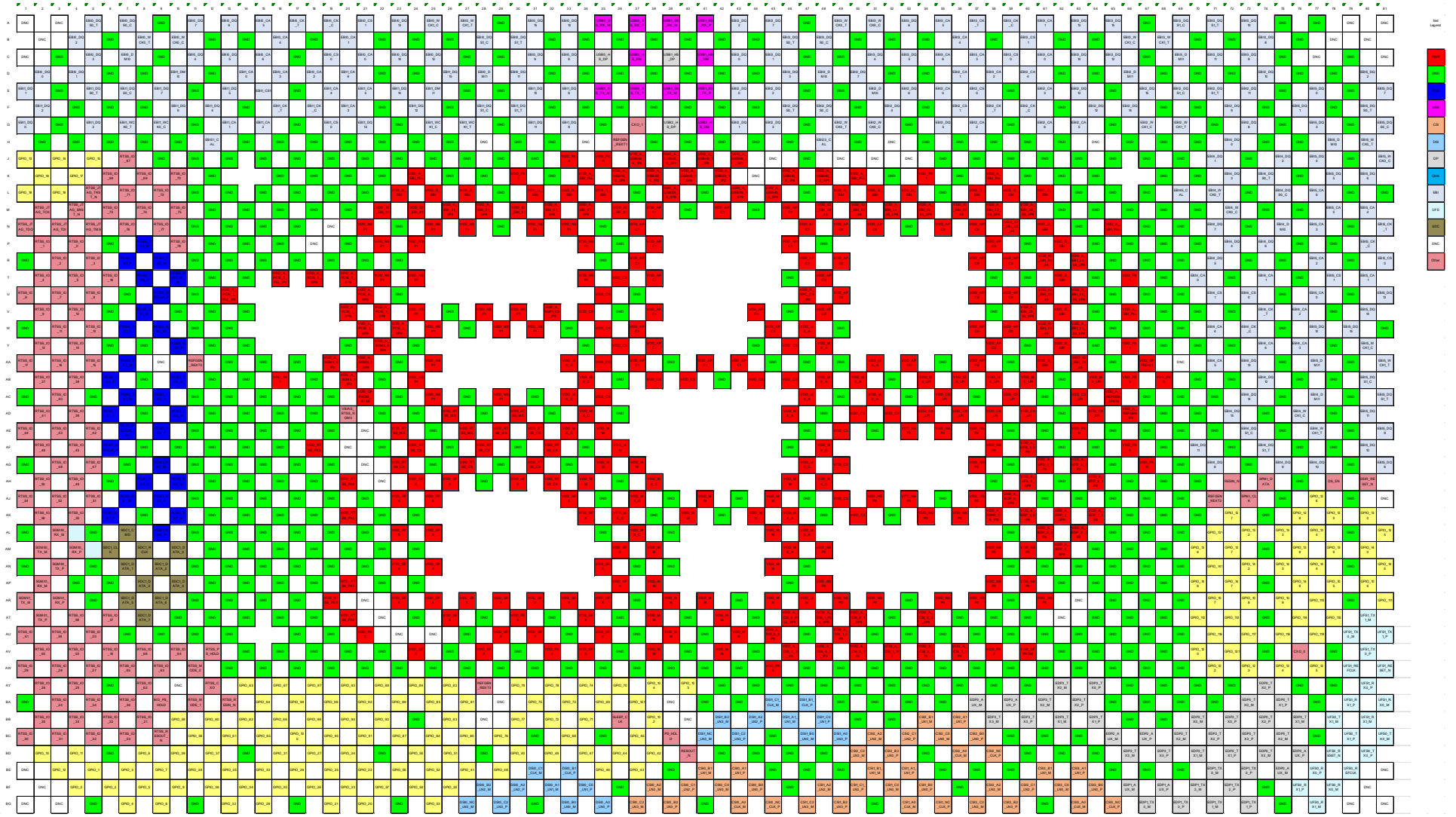


Figure 2-1 QCS9075 bottom pin assignments

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2.3 Pin descriptions

Table 2-2 Pin descriptions – primary pins

Pin no.	Pin name	Pad voltage	Pad type	Functional description
BG45	CSI0_NC_CLK_P	–	AI	MIPI CSI 0 (D-PHY), differential clock – plus MIPI CSI 0 (C-PHY), no connect
BG43	CSI0_A0_CLK_M	–	AI	MIPI CSI 0 (D-PHY), differential clock – minus MIPI CSI 0 (C-PHY), trio lane 0 – A
BF44	CSI0_B0_LN0_P	–	AI	MIPI CSI 0 (D-PHY), differential lane 0 – plus MIPI CSI 0 (C-PHY), trio lane 0 – B
BF42	CSI0_C0_LN0_M	–	AI	MIPI CSI 0 (D-PHY), differential lane 0 – minus MIPI CSI 0 (C-PHY), trio lane 0 – C
BE43	CSI0_A1_LN1_P	–	AI	MIPI CSI 0 (D-PHY), differential lane 1 – plus MIPI CSI 0 (C-PHY), trio lane 1 – A
BE41	CSI0_B1_LN1_M	–	AI	MIPI CSI 0 (D-PHY), differential lane 1 – minus MIPI CSI 0 (C-PHY), trio lane 1 – B
BF40	CSI0_C1_LN2_P	–	AI	MIPI CSI 0 (D-PHY), differential lane 2 – plus MIPI CSI 0 (C-PHY), trio lane 1 – C
BF38	CSI0_A2_LN2_M	–	AI	MIPI CSI 0 (D-PHY), differential lane 2 – minus MIPI CSI 0 (C-PHY), trio lane 2 – A
BG39	CSI0_B2_LN3_P	–	AI	MIPI CSI 0 (D-PHY), differential lane 3 – plus MIPI CSI 0 (C-PHY), trio lane 2 – B
BG37	CSI0_C2_LN3_M	–	AI	MIPI CSI 0 (D-PHY), differential lane 3 – minus MIPI CSI 0 (C-PHY), trio lane 2 – C
BG55	CSI1_NC_CLK_P	–	AI	MIPI CSI 1 (D-PHY), differential clock – plus MIPI CSI 1 (C-PHY), no connect
BG53	CSI1_A0_CLK_M	–	AI	MIPI CSI 1 (D-PHY), differential clock – minus MIPI CSI 1 (C-PHY), trio lane 0 – A
BF54	CSI1_B0_LN0_P	–	AI	MIPI CSI 1 (D-PHY), differential lane 0 – plus MIPI CSI 1 (C-PHY), trio lane 0 – B
BF52	CSI1_C0_LN0_M	–	AI	MIPI CSI 1 (D-PHY), differential lane 0 – minus MIPI CSI 1 (C-PHY), trio lane 0 – C
BE53	CSI1_A1_LN1_P	–	AI	MIPI CSI 1 (D-PHY), differential lane 1 – plus MIPI CSI 1 (C-PHY), trio lane 1 – A
BE51	CSI1_B1_LN1_M	–	AI	MIPI CSI 1 (D-PHY), differential lane 1 – minus MIPI CSI 1 (C-PHY), trio lane 1 – B
BF50	CSI1_C1_LN2_P	–	AI	MIPI CSI 1 (D-PHY), differential lane 2 – plus MIPI CSI 1 (C-PHY), trio lane 1 – C
BF48	CSI1_A2_LN2_M	–	AI	MIPI CSI 1 (D-PHY), differential lane 2 – minus MIPI CSI 1 (C-PHY), trio lane 2 – A
BG49	CSI1_B2_LN3_P	–	AI	MIPI CSI 1 (D-PHY), differential lane 3 – plus MIPI CSI 1 (C-PHY), trio lane 2 – B
BG47	CSI1_C2_LN3_M	–	AI	MIPI CSI 1 (D-PHY), differential lane 3 – minus MIPI CSI 1 (C-PHY), trio lane 2 – C
BD58	CSI2_NC_CLK_P	–	AI	MIPI CSI 2 (D-PHY), differential clock – plus MIPI CSI 2 (C-PHY), no connect
BD56	CSI2_A0_CLK_M	–	AI	MIPI CSI 2 (D-PHY), differential clock – minus MIPI CSI 2 (C-PHY), trio lane 0 – A

Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
BC57	CSI2_B0_LN0_P	–	AI	MIPI CSI 2 (D-PHY), differential lane 0 – plus MIPI CSI 2 (C-PHY), trio lane 0 – B
BC55	CSI2_C0_LN0_M	–	AI	MIPI CSI 2 (D-PHY), differential lane 0 – minus MIPI CSI 2 (C-PHY), trio lane 0 – C
BB56	CSI2_A1_LN1_P	–	AI	MIPI CSI 2 (D-PHY), differential lane 1 – plus MIPI CSI 2 (C-PHY), trio lane 1 – A
BB54	CSI2_B1_LN1_M	–	AI	MIPI CSI 2 (D-PHY), differential lane 1 – minus MIPI CSI 2 (C-PHY), trio lane 1 – B
BC53	CSI2_C1_LN2_P	–	AI	MIPI CSI 2 (D-PHY), differential lane 2 – plus MIPI CSI 2 (C-PHY), trio lane 1 – C
BC51	CSI2_A2_LN2_M	–	AI	MIPI CSI 2 (D-PHY), differential lane 2 – minus MIPI CSI 2 (C-PHY), trio lane 2 – A
BD52	CSI2_B2_LN3_P	–	AI	MIPI CSI 2 (D-PHY), differential lane 3 – plus MIPI CSI 2 (C-PHY), trio lane 2 – B
BD50	CSI2_C2_LN3_M	–	AI	MIPI CSI 2 (D-PHY), differential lane 3 – minus MIPI CSI 2 (C-PHY), trio lane 2 – C
BG65	CSI3_NC_CLK_P	–	AI	MIPI CSI 3 (D-PHY), differential clock – plus MIPI CSI 3 (C-PHY), no connect
BG63	CSI3_A0_CLK_M	–	AI	MIPI CSI 3 (D-PHY), differential clock – minus MIPI CSI 3 (C-PHY), trio lane 0 – A
BF64	CSI3_B0_LN0_P	–	AI	MIPI CSI 3 (D-PHY), differential lane 0 – plus MIPI CSI 3 (C-PHY), trio lane 0 – B
BF62	CSI3_C0_LN0_M	–	AI	MIPI CSI 3 (D-PHY), differential lane 0 – minus MIPI CSI 3 (C-PHY), trio lane 0 – C
BE63	CSI3_A1_LN1_P	–	AI	MIPI CSI 3 (D-PHY), differential lane 1 – plus MIPI CSI 3 (C-PHY), trio lane 1 – A
BE61	CSI3_B1_LN1_M	–	AI	MIPI CSI 3 (D-PHY), differential lane 1 – minus MIPI CSI 3 (C-PHY), trio lane 1 – B
BF60	CSI3_C1_LN2_P	–	AI	MIPI CSI 3 (D-PHY), differential lane 2 – plus MIPI CSI 3 (C-PHY), trio lane 1 – C
BF58	CSI3_A2_LN2_M	–	AI	MIPI CSI 3 (D-PHY), differential lane 2 – minus MIPI CSI 3 (C-PHY), trio lane 2 – A
BG59	CSI3_B2_LN3_P	–	AI	MIPI CSI 3 (D-PHY), differential lane 3 – plus MIPI CSI 3 (C-PHY), trio lane 2 – B
BG57	CSI3_C2_LN3_M	–	AI	MIPI CSI 3 (D-PHY), differential lane 3 – minus MIPI CSI 3 (C-PHY), trio lane 2 – C
AV76	CXO_0	PX_11	DI	Core crystal oscillator 0
G37	CXO_1	PX_11	DI	Core crystal oscillator 1
AH80	DDR_RESET_N	PX_1	DO	LPDDRx reset (shared by EBIs)
BG35	DSI0_A0_LN0_P	–	AO	MIPI DSI 0 (D-PHY), differential lane 0 – plus MIPI DSI 0 (C-PHY), trio lane 0 – A
BG33	DSI0_B0_LN0_M	–	AO	MIPI DSI 0 (D-PHY), differential lane 0 – minus MIPI DSI 0 (C-PHY), trio lane 0 – B
BF34	DSI0_C0_LN1_P	–	AO	MIPI DSI 0 (D-PHY), differential lane 1 – plus MIPI DSI 0 (C-PHY), trio lane 0 – C
BF32	DSI0_A1_LN1_M	–	AO	MIPI DSI 0 (D-PHY), differential lane 1 – minus MIPI DSI 0 (C-PHY), trio lane 1 – A

Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
BE33	DSI0_B1_CLK_P	–	AO	MIPI DSI 0 (D-PHY), differential clock – P – plus MIPI DSI 0 (C-PHY), trio lane 1 – B
BE31	DSI0_C1_CLK_M	–	AO	MIPI DSI 0 (D-PHY), differential clock – M – minus MIPI DSI 0 (C-PHY), trio lane 1 – C
BF30	DSI0_A2_LN2_P	–	AO	MIPI DSI 0 (D-PHY), differential lane 2 – plus MIPI DSI 0 (C-PHY), trio lane 2 – A
BF28	DSI0_B2_LN2_M	–	AO	MIPI DSI 0 (D-PHY), differential lane 2 – minus MIPI DSI 0 (C-PHY), trio lane 2 – B
BG29	DSI0_C2_LN3_P	–	AO	MIPI DSI 0 (D-PHY), differential lane 3 – plus MIPI DSI 0 (C-PHY), trio lane 2 – C
BG27	DSI0_NC_LN3_M	–	AO	MIPI DSI 0 (D-PHY), differential lane 3 – minus MIPI DSI 0 (C-PHY), no connect
BC49	DSI1_A0_LN0_P	–	AO	MIPI DSI 1 (D-PHY), differential lane 0 – plus MIPI DSI 1 (C-PHY), trio lane 0 – A
BC47	DSI1_B0_LN0_M	–	AO	MIPI DSI 1 (D-PHY), differential lane 0 – minus MIPI DSI 1 (C-PHY), trio lane 0 – B
BB48	DSI1_C0_LN1_P	–	AO	MIPI DSI 1 (D-PHY), differential lane 1 – plus MIPI DSI 1 (C-PHY), trio lane 0 – C
BB46	DSI1_A1_LN1_M	–	AO	MIPI DSI 1 (D-PHY), differential lane 1 – minus MIPI DSI 1 (C-PHY), trio lane 1 – A
BA47	DSI1_B1_CLK_P	–	AO	MIPI DSI 1 (D-PHY), differential clock – P – plus MIPI DSI 1 (C-PHY), trio lane 1 – B
BA45	DSI1_C1_CLK_M	–	AO	MIPI DSI 1 (D-PHY), differential clock – M – minusMIPI DSI 1 (C-PHY), trio lane 1 – C
BB44	DSI1_A2_LN2_P	–	AO	MIPI DSI 1 (D-PHY), differential lane 2 – plus MIPI DSI 1 (C-PHY), trio lane 2 – A
BB42	DSI1_B2_LN2_M	–	AO	MIPI DSI 1 (D-PHY), differential lane 2 – minus MIPI DSI 1 (C-PHY), trio lane 2 – B
BC43	DSI1_C2_LN3_P	–	AO	MIPI DSI 1 (D-PHY), differential lane 3 – plus MIPI DSI 1 (C-PHY), trio lane 2 – C
BC41	DSI1_NC_LN3_M	–	AO	MIPI DSI 1 (D-PHY), differential lane 3 – minus MIPI DSI 1 (C-PHY), no connect
AH78	DS_EN	PX_0	DI	Deep sleep handshake between PMIC and SoC
H12	EBI01_CAL	–	DO	EBI calibration resistor
C21	EBI0_CA0	–	DO	EBI0 LPDDR5 command/address bit 0
B20	EBI0_CA1	–	DO	EBI0 LPDDR5 command/address bit 1
D18	EBI0_CA2	–	DO	EBI0 LPDDR5 command/address bit 2
D16	EBI0_CA3	–	DO	EBI0 LPDDR5 command/address bit 3
B16	EBI0_CA4	–	DO	EBI0 LPDDR5 command/address bit 4
A15	EBI0_CA5	–	DO	EBI0 LPDDR5 command/address bit 5
C15	EBI0_CA6	–	DO	EBI0 LPDDR5 command/address bit 6
A19	EBI0_CK_C	–	DO	EBI0 LPDDR5 differential clock – minus
A17	EBI0_CK_T	–	DO	EBI0 LPDDR5 differential clock – plus
C19	EBI0_CS0	–	DO	EBI0 LPDDR5 chip select 0
A21	EBI0_CS1	–	DO	EBI0 LPDDR5 chip select 1

Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
C7	EBI0_DMI0	–	DO	EBI0 LPDDR5 data mask for byte 0
D28	EBI0_DMI1	–	DO	EBI0 LPDDR5 data mask for byte 1
D2	EBI0_DQ0	–	B	EBI0 LPDDR5 data bit 0
D4	EBI0_DQ1	–	B	EBI0 LPDDR5 data bit 1
B4	EBI0_DQ2	–	B	EBI0 LPDDR5 data bit 2
C5	EBI0_DQ3	–	B	EBI0 LPDDR5 data bit 3
C11	EBI0_DQ4	–	B	EBI0 LPDDR5 data bit 4
C13	EBI0_DQ5	–	B	EBI0 LPDDR5 data bit 5
A13	EBI0_DQ6	–	B	EBI0 LPDDR5 data bit 6
A11	EBI0_DQ7	–	B	EBI0 LPDDR5 data bit 7
C33	EBI0_DQ8	–	B	EBI0 LPDDR5 data bit 8
C31	EBI0_DQ9	–	B	EBI0 LPDDR5 data bit 9
A33	EBI0_DQ10	–	B	EBI0 LPDDR5 data bit 10
D30	EBI0_DQ11	–	B	EBI0 LPDDR5 data bit 11
C25	EBI0_DQ12	–	B	EBI0 LPDDR5 data bit 12
A23	EBI0_DQ13	–	B	EBI0 LPDDR5 data bit 13
C23	EBI0_DQ14	–	B	EBI0 LPDDR5 data bit 14
A31	EBI0_DQ15	–	B	EBI0 LPDDR5 data bit 15
A7	EBI0_DQS0_C	–	DI	EBI0 LPDDR5 differential read data strobe for byte 0 – minus
A5	EBI0_DQS0_T	–	DI	EBI0 LPDDR5 differential read data strobe for byte 0 – plus
B28	EBI0_DQS1_C	–	DI	EBI0 LPDDR5 differential read data strobe for byte 1 – minus
B30	EBI0_DQS1_T	–	DI	EBI0 LPDDR5 differential read data strobe for byte 1 – plus
B10	EBI0_WCK0_C	–	DO	EBI0 LPDDR5 differential write clock for byte 0 – minus
B8	EBI0_WCK0_T	–	DO	EBI0 LPDDR5 differential write clock for byte 0 – plus
A25	EBI0_WCK1_C	–	DO	EBI0 LPDDR5 differential write clock for byte 1 – minus
A27	EBI0_WCK1_T	–	DO	EBI0 LPDDR5 differential write clock for byte 1 – plus
D14	EBI1_CA0	–	DO	EBI1 LPDDR5 command/address bit 0
G13	EBI1_CA1	–	DO	EBI1 LPDDR5 command/address bit 1
G15	EBI1_CA2	–	DO	EBI1 LPDDR5 command/address bit 2
F20	EBI1_CA3	–	DO	EBI1 LPDDR5 command/address bit 3
E19	EBI1_CA4	–	DO	EBI1 LPDDR5 command/address bit 4
E21	EBI1_CA5	–	DO	EBI1 LPDDR5 command/address bit 5
D20	EBI1_CA6	–	DO	EBI1 LPDDR5 command/address bit 6
F18	EBI1_CK_C	–	DO	EBI1 LPDDR5 differential clock – minus

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Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
F16	EBI1_CK_T	–	DO	EBI1 LPDDR5 differential clock – plus
G19	EBI1_CS0	–	DO	EBI1 LPDDR5 chip select 0
E15	EBI1_CS1	–	DO	EBI1 LPDDR5 chip select 1
D10	EBI1_DMI0	–	DO	EBI1 LPDDR5 data mask for byte 0
E25	EBI1_DMI1	–	DO	EBI1 LPDDR5 data mask for byte 1
G1	EBI1_DQ0	–	B	EBI1 LPDDR5 data bit 0
E1	EBI1_DQ1	–	B	EBI1 LPDDR5 data bit 1
F2	EBI1_DQ2	–	B	EBI1 LPDDR5 data bit 2
G5	EBI1_DQ3	–	B	EBI1 LPDDR5 data bit 3
F12	EBI1_DQ4	–	B	EBI1 LPDDR5 data bit 4
E13	EBI1_DQ5	–	B	EBI1 LPDDR5 data bit 5
F10	EBI1_DQ6	–	B	EBI1 LPDDR5 data bit 6
E9	EBI1_DQ7	–	B	EBI1 LPDDR5 data bit 7
E33	EBI1_DQ8	–	B	EBI1 LPDDR5 data bit 8
G33	EBI1_DQ9	–	B	EBI1 LPDDR5 data bit 9
E31	EBI1_DQ10	–	B	EBI1 LPDDR5 data bit 10
G31	EBI1_DQ11	–	B	EBI1 LPDDR5 data bit 11
F24	EBI1_DQ12	–	B	EBI1 LPDDR5 data bit 12
G21	EBI1_DQ13	–	B	EBI1 LPDDR5 data bit 13
E23	EBI1_DQ14	–	B	EBI1 LPDDR5 data bit 14
D26	EBI1_DQ15	–	B	EBI1 LPDDR5 data bit 15
E7	EBI1_DQS0_C	–	DI	EBI1 LPDDR5 differential read data strobe for byte 0 – minus
E5	EBI1_DQS0_T	–	DI	EBI1 LPDDR5 differential read data strobe for byte 0 – plus
F28	EBI1_DQS1_C	–	DI	EBI1 LPDDR5 differential read data strobe for byte 1 – minus
F30	EBI1_DQS1_T	–	DI	EBI1 LPDDR5 differential read data strobe for byte 1 – plus
G9	EBI1_WCK0_C	–	DO	EBI1 LPDDR5 differential write clock for byte 0 – minus
G7	EBI1_WCK0_T	–	DO	EBI1 LPDDR5 differential write clock for byte 0 – plus
G25	EBI1_WCK1_C	–	DO	EBI1 LPDDR5 differential write clock for byte 1 – minus
G27	EBI1_WCK1_T	–	DO	EBI1 LPDDR5 differential write clock for byte 1 – plus
H48	EBI23_CAL	–	DO	EBI calibration resistor
E55	EBI2_CA0	–	DO	EBI2 LPDDR5 command/address bit 0
D56	EBI2_CA1	–	DO	EBI2 LPDDR5 command/address bit 1
G57	EBI2_CA2	–	DO	EBI2 LPDDR5 command/address bit 2
E61	EBI2_CA3	–	DO	EBI2 LPDDR5 command/address bit 3

Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
D60	EBI2_CA4	–	DO	EBI2 LPDDR5 command/address bit 4
G63	EBI2_CA5	–	DO	EBI2 LPDDR5 command/address bit 5
G61	EBI2_CA6	–	DO	EBI2 LPDDR5 command/address bit 6
F60	EBI2_CK_C	–	DO	EBI2 LPDDR5 differential clock – minus
F58	EBI2_CK_T	–	DO	EBI2 LPDDR5 differential clock – plus
E57	EBI2_CS0	–	DO	EBI2 LPDDR5 chip select 0
F56	EBI2_CS1	–	DO	EBI2 LPDDR5 chip select 1
E51	EBI2_DMI0	–	DO	EBI2 LPDDR5 data mask for byte 0
D66	EBI2_DMI1	–	DO	EBI2 LPDDR5 data mask for byte 1
E43	EBI2_DQ0	–	B	EBI2 LPDDR5 data bit 0
G43	EBI2_DQ1	–	B	EBI2 LPDDR5 data bit 1
E45	EBI2_DQ2	–	B	EBI2 LPDDR5 data bit 2
G45	EBI2_DQ3	–	B	EBI2 LPDDR5 data bit 3
F52	EBI2_DQ4	–	B	EBI2 LPDDR5 data bit 4
G55	EBI2_DQ5	–	B	EBI2 LPDDR5 data bit 5
E53	EBI2_DQ6	–	B	EBI2 LPDDR5 data bit 6
D50	EBI2_DQ7	–	B	EBI2 LPDDR5 data bit 7
G73	EBI2_DQ8	–	B	EBI2 LPDDR5 data bit 8
F72	EBI2_DQ9	–	B	EBI2 LPDDR5 data bit 9
D74	EBI2_DQ10	–	B	EBI2 LPDDR5 data bit 10
E73	EBI2_DQ11	–	B	EBI2 LPDDR5 data bit 11
F64	EBI2_DQ12	–	B	EBI2 LPDDR5 data bit 12
E63	EBI2_DQ13	–	B	EBI2 LPDDR5 data bit 13
F66	EBI2_DQ14	–	B	EBI2 LPDDR5 data bit 14
E67	EBI2_DQ15	–	B	EBI2 LPDDR5 data bit 15
F48	EBI2_DQS0_C	–	DI	EBI2 LPDDR5 differential read data strobe for byte 0 – minus
F46	EBI2_DQS0_T	–	DI	EBI2 LPDDR5 differential read data strobe for byte 0 – plus
E69	EBI2_DQS1_C	–	DI	EBI2 LPDDR5 differential read data strobe for byte 1 – minus
E71	EBI2_DQS1_T	–	DI	EBI2 LPDDR5 differential read data strobe for byte 1 – plus
G51	EBI2_WCK0_C	–	DO	EBI2 LPDDR5 differential write clock for byte 0 – minus
G49	EBI2_WCK0_T	–	DO	EBI2 LPDDR5 differential write clock for byte 0 – plus
G67	EBI2_WCK1_C	–	DO	EBI2 LPDDR5 differential write clock for byte 1 – minus
G69	EBI2_WCK1_T	–	DO	EBI2 LPDDR5 differential write clock for byte 1 – plus
C61	EBI3_CA0	–	DO	EBI3 LPDDR5 command/address bit 0

Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
A61	EBI3_CA1	–	DO	EBI3 LPDDR5 command/address bit 1
D58	EBI3_CA2	–	DO	EBI3 LPDDR5 command/address bit 2
C57	EBI3_CA3	–	DO	EBI3 LPDDR5 command/address bit 3
B56	EBI3_CA4	–	DO	EBI3 LPDDR5 command/address bit 4
A55	EBI3_CA5	–	DO	EBI3 LPDDR5 command/address bit 5
C55	EBI3_CA6	–	DO	EBI3 LPDDR5 command/address bit 6
A59	EBI3_CK_C	–	DO	EBI3 LPDDR5 differential clock – minus
A57	EBI3_CK_T	–	DO	EBI3 LPDDR5 differential clock – plus
C59	EBI3_CS0	–	DO	EBI3 LPDDR5 chip select 0
B60	EBI3_CS1	–	DO	EBI3 LPDDR5 chip select 1
D48	EBI3_DMI0	–	DO	EBI3 LPDDR5 data mask for byte 0
C69	EBI3_DMI1	–	DO	EBI3 LPDDR5 data mask for byte 1
C43	EBI3_DQ0	–	B	EBI3 LPDDR5 data bit 0
C45	EBI3_DQ1	–	B	EBI3 LPDDR5 data bit 1
A43	EBI3_DQ2	–	B	EBI3 LPDDR5 data bit 2
D46	EBI3_DQ3	–	B	EBI3 LPDDR5 data bit 3
C51	EBI3_DQ4	–	B	EBI3 LPDDR5 data bit 4
C53	EBI3_DQ5	–	B	EBI3 LPDDR5 data bit 5
A53	EBI3_DQ6	–	B	EBI3 LPDDR5 data bit 6
A45	EBI3_DQ7	–	B	EBI3 LPDDR5 data bit 7
B74	EBI3_DQ8	–	B	EBI3 LPDDR5 data bit 8
C73	EBI3_DQ9	–	B	EBI3 LPDDR5 data bit 9
A73	EBI3_DQ10	–	B	EBI3 LPDDR5 data bit 10
C71	EBI3_DQ11	–	B	EBI3 LPDDR5 data bit 11
C65	EBI3_DQ12	–	B	EBI3 LPDDR5 data bit 12
A63	EBI3_DQ13	–	B	EBI3 LPDDR5 data bit 13
C63	EBI3_DQ14	–	B	EBI3 LPDDR5 data bit 14
A65	EBI3_DQ15	–	B	EBI3 LPDDR5 data bit 15
B48	EBI3_DQS0_C	–	DI	EBI3 LPDDR5 differential read data strobe for byte 0 – minus
B46	EBI3_DQS0_T	–	DI	EBI3 LPDDR5 differential read data strobe for byte 0 – plus
A69	EBI3_DQS1_C	–	DI	EBI3 LPDDR5 differential read data strobe for byte 1 – minus
A71	EBI3_DQS1_T	–	DI	EBI3 LPDDR5 differential read data strobe for byte 1 – plus
A51	EBI3_WCK0_C	–	DO	EBI3 LPDDR5 differential write clock for byte 0 – minus
A49	EBI3_WCK0_T	–	DO	EBI3 LPDDR5 differential write for byte 0 – plus
B66	EBI3_WCK1_C	–	DO	EBI3 LPDDR5 differential write clock for byte 1 – minus

Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
B68	EBI3_WCK1_T	–	DO	EBI3 LPDDR5 differential write clock for byte 1 – plus
L69	EBI45_CAL	–	DO	EBI calibration resistor
T70	EBI4_CA0	–	DO	EBI4 LPDDR5 command/address bit 0
T74	EBI4_CA1	–	DO	EBI4 LPDDR5 command/address bit 1
V76	EBI4_CA2	–	DO	EBI4 LPDDR5 command/address bit 2
Y76	EBI4_CA3	–	DO	EBI4 LPDDR5 command/address bit 3
W71	EBI4_CA4	–	DO	EBI4 LPDDR5 command/address bit 4
AA71	EBI4_CA5	–	DO	EBI4 LPDDR5 command/address bit 5
Y74	EBI4_CA6	–	DO	EBI4 LPDDR5 command/address bit 6
W73	EBI4_CK_C	–	DO	EBI4 LPDDR5 differential clock – minus
V74	EBI4_CK_T	–	DO	EBI4 LPDDR5 differential clock – plus
U73	EBI4_CS0	–	DO	EBI4 LPDDR5 chip select 0
U71	EBI4_CS1	–	DO	EBI4 LPDDR5 chip select 1
N75	EBI4_DMI0	–	DO	EBI4 LPDDR5 data mask for byte 0
AC77	EBI4_DMI1	–	DO	EBI4 LPDDR5 data mask for byte 1
H72	EBI4_DQ0	–	B	EBI4 LPDDR5 data bit 0
J71	EBI4_DQ1	–	B	EBI4 LPDDR5 data bit 1
J75	EBI4_DQ2	–	B	EBI4 LPDDR5 data bit 2
K72	EBI4_DQ3	–	B	EBI4 LPDDR5 data bit 3
P72	EBI4_DQ4	–	B	EBI4 LPDDR5 data bit 4
R71	EBI4_DQ5	–	B	EBI4 LPDDR5 data bit 5
P74	EBI4_DQ6	–	B	EBI4 LPDDR5 data bit 6
N71	EBI4_DQ7	–	B	EBI4 LPDDR5 data bit 7
AG71	EBI4_DQ8	–	B	EBI4 LPDDR5 data bit 8
AG75	EBI4_DQ9	–	B	EBI4 LPDDR5 data bit 9
AG77	EBI4_DQ10	–	B	EBI4 LPDDR5 data bit 10
AF70	EBI4_DQ11	–	B	EBI4 LPDDR5 data bit 11
AB74	EBI4_DQ12	–	B	EBI4 LPDDR5 data bit 12
AA73	EBI4_DQ13	–	B	EBI4 LPDDR5 data bit 13
AC73	EBI4_DQ14	–	B	EBI4 LPDDR5 data bit 14
AD72	EBI4_DQ15	–	B	EBI4 LPDDR5 data bit 15
L75	EBI4_DQS0_C	–	DI	EBI4 LPDDR5 differential read data strobe for byte 0 – minus
K74	EBI4_DQS0_T	–	DI	EBI4 LPDDR5 differential read data strobe for byte 0 – plus
AE73	EBI4_DQS1_C	–	DI	EBI4 LPDDR5 differential read data strobe for byte 1 – minus
AF74	EBI4_DQS1_T	–	DI	EBI4 LPDDR5 differential read data strobe for byte 1 – plus

Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
M72	EBI4_WCK0_C	–	DO	EBI4 LPDDR5 differential write clock for byte 0 – minus
L71	EBI4_WCK0_T	–	DO	EBI4 LPDDR5 differential write clock for byte 0 – plus
AD76	EBI4_WCK1_C	–	DO	EBI4 LPDDR5 differential write clock for byte 1 – minus
AE77	EBI4_WCK1_T	–	DO	EBI4 LPDDR5 differential write clock for byte 1 – plus
U77	EBI5_CA0	–	DO	EBI5 LPDDR5 command/address bit 0
T80	EBI5_CA1	–	DO	EBI5 LPDDR5 command/address bit 1
R77	EBI5_CA2	–	DO	EBI5 LPDDR5 command/address bit 2
N77	EBI5_CA3	–	DO	EBI5 LPDDR5 command/address bit 3
M80	EBI5_CA4	–	DO	EBI5 LPDDR5 command/address bit 4
M78	EBI5_CA5	–	DO	EBI5 LPDDR5 command/address bit 5
L77	EBI5_CA6	–	DO	EBI5 LPDDR5 command/address bit 6
P80	EBI5_CK_C	–	DO	EBI5 LPDDR5 differential clock – minus
N81	EBI5_CK_T	–	DO	EBI5 LPDDR5 differential clock – plus
R81	EBI5_CS0	–	DO	EBI5 LPDDR5 chip select 0
T78	EBI5_CS1	–	DO	EBI5 LPDDR5 chip select 1
H78	EBI5_DMI0	–	DO	EBI5 LPDDR5 data mask for byte 0
AA77	EBI5_DMI1	–	DO	EBI5 LPDDR5 data mask for byte 1
E77	EBI5_DQ0	–	B	EBI5 LPDDR5 data bit 0
F76	EBI5_DQ1	–	B	EBI5 LPDDR5 data bit 1
D80	EBI5_DQ2	–	B	EBI5 LPDDR5 data bit 2
G77	EBI5_DQ3	–	B	EBI5 LPDDR5 data bit 3
J77	EBI5_DQ4	–	B	EBI5 LPDDR5 data bit 4
K78	EBI5_DQ5	–	B	EBI5 LPDDR5 data bit 5
K80	EBI5_DQ6	–	B	EBI5 LPDDR5 data bit 6
E81	EBI5_DQ7	–	B	EBI5 LPDDR5 data bit 7
AG81	EBI5_DQ8	–	B	EBI5 LPDDR5 data bit 8
AE81	EBI5_DQ9	–	B	EBI5 LPDDR5 data bit 9
AF80	EBI5_DQ10	–	B	EBI5 LPDDR5 data bit 10
AD80	EBI5_DQ11	–	B	EBI5 LPDDR5 data bit 11
W77	EBI5_DQ12	–	B	EBI5 LPDDR5 data bit 12
U81	EBI5_DQ13	–	B	EBI5 LPDDR5 data bit 13
V80	EBI5_DQ14	–	B	EBI5 LPDDR5 data bit 14
W79	EBI5_DQ15	–	B	EBI5 LPDDR5 data bit 15
G81	EBI5_DQS0_C	–	DI	EBI5 LPDDR5 differential read data strobe for byte 0 – minus
AB80	EBI5_DQS1_C	–	DI	EBI5 LPDDR5 differential read data strobe for byte 1 – minus

Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
F80	EBI5_DQS0_T	–	DI	EBI5 LPDDR5 differential read data strobe for byte 0 – plus
AC81	EBI5_DQS1_T	–	DI	EBI5 LPDDR5 differential read data strobe for byte 1 – plus
J81	EBI5_WCK0_C	–	DO	EBI5 LPDDR5 differential write clock for byte 0 – minus
Y80	EBI5_WCK1_C	–	DO	EBI5 LPDDR5 differential write clock for byte 1 – minus
H80	EBI5_WCK0_T	–	DO	EBI5 LPDDR5 differential write clock for byte 0 – plus
AA81	EBI5_WCK1_T	–	DO	EBI5 LPDDR5 differential write clock for byte 1 – plus
BE75	EDP0_AUX_M	–	AI, AO	eDP/DP 0 auxiliary channel – minus
BD76	EDP0_AUX_P	–	AI, AO	eDP/DP 0 auxiliary channel – plus
BA73	EDP0_TX0_M	–	AO	eDP/DP 0 transmit channel 0 – minus
AY74	EDP0_TX0_P	–	AO	eDP/DP 0 transmit channel 0 – plus
BB76	EDP0_TX1_M	–	AO	eDP/DP 0 transmit channel 1 – minus
BA75	EDP0_TX1_P	–	AO	eDP/DP 0 transmit channel 1 – plus
BC75	EDP0_TX2_M	–	AO	eDP/DP 0 transmit channel 2 – minus
BB74	EDP0_TX2_P	–	AO	eDP/DP 0 transmit channel 2 – plus
BD74	EDP0_TX3_M	–	AO	eDP/DP 0 transmit channel 3 – minus
BC73	EDP0_TX3_P	–	AO	eDP/DP 0 transmit channel 3 – plus
BF66	EDP1_AUX_M	–	AI, AO	eDP/DP 1 auxiliary channel – minus
BF68	EDP1_AUX_P	–	AI, AO	eDP/DP 1 auxiliary channel – plus
BE71	EDP1_TX0_M	–	AO	eDP/DP 1 transmit channel 0 – minus
BE73	EDP1_TX0_P	–	AO	eDP/DP 1 transmit channel 0 – plus
BG71	EDP1_TX1_M	–	AO	eDP/DP 1 transmit channel 1 – minus
BG73	EDP1_TX1_P	–	AO	eDP/DP 1 transmit channel 1 – plus
BF70	EDP1_TX2_M	–	AO	eDP/DP 1 transmit channel 2 – minus
BF72	EDP1_TX2_P	–	AO	eDP/DP 1 transmit channel 2 – plus
BG67	EDP1_TX3_M	–	AO	eDP/DP 1 transmit channel 3 – minus
BG69	EDP1_TX3_P	–	AO	eDP/DP 1 transmit channel 3 – plus
BC65	EDP2_AUX_M	–	AI, AO	eDP/DP 2 auxiliary channel – minus
BC67	EDP2_AUX_P	–	AI, AO	eDP/DP 2 auxiliary channel – plus
BB70	EDP2_TX0_M	–	AO	eDP/DP 2 transmit channel 0 – minus
BB72	EDP2_TX0_P	–	AO	eDP/DP 2 transmit channel 0 – plus
BD70	EDP2_TX1_M	–	AO	eDP/DP 2 transmit channel 1 – minus
BD72	EDP2_TX1_P	–	AO	eDP/DP 2 transmit channel 1 – plus
BC69	EDP2_TX2_M	–	AO	eDP/DP 2 transmit channel 2 – minus
BC71	EDP2_TX2_P	–	AO	eDP/DP 2 transmit channel 2 – plus
BD66	EDP2_TX3_M	–	AO	eDP/DP 2 transmit channel 3 – minus

Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
BD68	EDP2_TX3_P	–	AO	eDP/DP 2 transmit channel 3 – plus
BA57	EDP3_AUX_M	–	AI, AO	eDP/DP 3 auxiliary channel – minus
BA59	EDP3_AUX_P	–	AI, AO	eDP/DP 3 auxiliary channel – plus
AY62	EDP3_TX0_M	–	AO	eDP/DP 3 transmit channel 0 – minus
AY64	EDP3_TX0_P	–	AO	eDP/DP 3 transmit channel 0 – plus
BB62	EDP3_TX1_M	–	AO	eDP/DP 3 transmit channel 1 – minus
BB64	EDP3_TX1_P	–	AO	eDP/DP 3 transmit channel 1 – plus
BA61	EDP3_TX2_M	–	AO	eDP/DP 3 transmit channel 2 – minus
BA63	EDP3_TX2_P	–	AO	eDP/DP 3 transmit channel 2 – plus
BB58	EDP3_TX3_M	–	AO	eDP/DP 3 transmit channel 3 – minus
BB60	EDP3_TX3_P	–	AO	eDP/DP 3 transmit channel 3 – plus
BA9	MD_PS_HOLD	RTSS_PX_3 _BPP	DI	Power-supply hold signal from main domain
T10	PCIE0_REFCLK_M	–	AI, AO	PCIe 0 Gen 4 reference clock – minus
U9	PCIE0_REFCLK_P	–	AI, AO	PCIe 0 Gen 4 reference clock – plus
W9	PCIE0_RX0_M	–	AI	PCIe 0 Gen 4 receive – minus
Y10	PCIE0_RX0_P	–	AI	PCIe 0 Gen 4 receive – plus
V8	PCIE0_RX1_M	–	AI	PCIe 0 Gen 4 receive – minus
W7	PCIE0_RX1_P	–	AI	PCIe 0 Gen 4 receive – plus
R9	PCIE0_TX0_M	–	AO	PCIe 0 Gen 4 transmit – minus
T8	PCIE0_TX0_P	–	AO	PCIe 0 Gen 4 transmit – plus
P8	PCIE0_TX1_M	–	AO	PCIe 0 Gen 4 transmit – minus
R7	PCIE0_TX1_P	–	AO	PCIe 0 Gen 4 transmit – plus
AE7	PCIE1_REFCLK_M	–	AI, AO	PCIe 1 Gen 4 reference clock – minus
AF6	PCIE1_REFCLK_P	–	AI, AO	PCIe 1 Gen 4 reference clock – plus
AK10	PCIE1_RX0_M	–	AI	PCIe 1 Gen 4 receive – minus
AL9	PCIE1_RX0_P	–	AI	PCIe 1 Gen 4 receive – plus
AJ7	PCIE1_RX1_M	–	AI	PCIe 1 Gen 4 receive – minus
AK6	PCIE1_RX1_P	–	AI	PCIe 1 Gen 4 receive – plus
AH10	PCIE1_RX2_M	–	AI	PCIe 1 Gen 4 receive – minus
AJ9	PCIE1_RX2_P	–	AI	PCIe 1 Gen 4 receive – plus
AG9	PCIE1_RX3_M	–	AI	PCIe 1 Gen 4 receive – minus
AH8	PCIE1_RX3_P	–	AI	PCIe 1 Gen 4 receive – plus
AD10	PCIE1_TX0_M	–	AO	PCIe 1 Gen 4 transmit – minus
AE9	PCIE1_TX0_P	–	AO	PCIe 1 Gen 4 transmit – plus
AC7	PCIE1_TX1_M	–	AO	PCIe 1 Gen 4 transmit – minus
AD6	PCIE1_TX1_P	–	AO	PCIe 1 Gen 4 transmit – plus
AB10	PCIE1_TX2_M	–	AO	PCIe 1 Gen 4 transmit – minus
AC9	PCIE1_TX2_P	–	AO	PCIe 1 Gen 4 transmit – plus

Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
AA7	PCIE1_TX3_M	–	AO	PCIe 1 Gen 4 transmit – minus
AB6	PCIE1_TX3_P	–	AO	PCIe 1 Gen 4 transmit – plus
BC39	PS_HOLD	PX_3_BPP	DO	Main domain power-supply hold signal to PMIC
AA11	REFGEN_REXT0	–	AI	High-speed interface – external resistor 0
H36	REFGEN_REXT1	–	AI	High-speed interface – external resistor 1
AJ71	REFGEN_REXT2	–	AI	High-speed interface – external resistor 2
AY28	REFGEN_REXT3	–	AI	High-speed interface – external resistor 3
AH72	RESIN_N	PX_0	DI	Main domain reset input
BD40	RESOUT_N	PX_3	DO	Main domain reset output
AY12	RTSS_CXO	RTSS_PX_11	DI	Core crystal oscillator for RTSS domain (digital 19.2 Hz system clock)
M4	RTSS_JTAG_SRST_N	RTSS_PX_3	DI-PU	RTSS domain JTAG reset for debug
M2	RTSS_JTAG_TCK	RTSS_PX_3	DI-PU	RTSS domain JTAG clock input
N3	RTSS_JTAG_TDI	RTSS_PX_3	DI-PU:nppdkp	RTSS domain JTAG data input
N1	RTSS_JTAG_TDO	RTSS_PX_3	DO-Z	RTSS domain JTAG data output
N5	RTSS_JTAG_TMS	RTSS_PX_3	DI-PU:nppdkp	RTSS domain JTAG mode select input
L5	RTSS_JTAG_TRST_N	RTSS_PX_3	DI-B-PD:nppukp	RTSS domain JTAG reset
AW11	RTSS_MODE_0	RTSS_PX_3	DI-S PD	Mode control bits [1:0] 00 for mission mode 11 for boundary scan mode
BA11	RTSS_MODE_1	RTSS_PX_3	DI-S PD	
AV12	RTSS_PS_HOLD	RTSS_PX_3	DO	Power-supply hold signal from RTSS
BA13	RTSS_RESIN_N	RTSS_PX_0	DI	RTSS domain reset input
BC9	RTSS_RESOUT_N	RTSS_PX_3	DO	RTSS domain reset output
AL3	SGMII0_RX_M	–	AI	SGMII interface 0 serial data Rx – minus
AM4	SGMII0_RX_P	–	AI	SGMII interface 0 serial data Rx – plus
AM2	SGMII0_TX_M	–	AO	SGMII interface 0 serial data Tx – minus
AN3	SGMII0_TX_P	–	AO	SGMII interface 0 serial data Tx – plus
AP2	SGMII1_RX_M	–	AI	SGMII interface 1 serial data Rx – minus
AR3	SGMII1_RX_P	–	AI	SGMII interface 1 serial data Rx – plus
AR1	SGMII1_TX_M	–	AO	SGMII interface 1 serial data Tx – minus
AT2	SGMII1_TX_P	–	AO	SGMII interface 1 serial data Tx – plus
BB36	SLEEP_CLK	PX_3	DI	Sleep clock
AJ73	SPMI_CLK	PX_0_BPP	B	Slave and PBUS interface for PMICs – clock
AH74	SPMI_DATA	PX_0_BPP	B	Slave and PBUS interface for PMICs – data
BE79	UFS0_REFCLK	PX_9	DO	UFS 0 reference clock

Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
BD78	UFS0_RESET_N	PX_9	DO	UFS 0 reset
BF78	UFS0_RX0_M	–	AI	UFS 0 receive 0 – minus
BE77	UFS0_RX0_P	–	AI	UFS 0 receive 0 – plus
BG77	UFS0_RX1_M	–	AI	UFS 0 receive 1 – minus
BF76	UFS0_RX1_P	–	AI	UFS 0 receive 1 – plus
BC81	UFS0_TX0_M	–	AO	UFS 0 transmit 0 – minus
BD80	UFS0_TX0_P	–	AO	UFS 0 transmit 0 – plus
BB78	UFS0_TX1_M	–	AO	UFS 0 transmit 1 – minus
BC79	UFS0_TX1_P	–	AO	UFS 0 transmit 1 – plus
AW79	UFS1_REFCLK	PX_10	DO	UFS 1 reference clock
AW81	UFS1_RESET_N	PX_10	DO	UFS 1 reset
BA81	UFS1_RX0_M	–	AI	UFS 1 receive 0 – minus
AY80	UFS1_RX0_P	–	AI	UFS 1 receive 0 – plus
BB80	UFS1_RX1_M	–	AI	UFS 1 receive 1 – minus
BA79	UFS1_RX1_P	–	AI	UFS 1 receive 1 – plus
AU79	UFS1_TX0_M	–	AO	UFS 1 transmit 0 – minus
AV80	UFS1_TX0_P	–	AO	UFS 1 transmit 0 – plus
AT80	UFS1_TX1_M	–	AO	UFS 1 transmit 1 – minus
AU81	UFS1_TX1_P	–	AO	UFS 1 transmit 1 – plus
C37	USB0_HS_DM	–	AI, AO	USB 0 high-speed data – minus
C35	USB0_HS_DP	–	AI, AO	USB 0 high-speed data – plus
A35	USB0_SS_RX_M	–	AI	USB 0 super-speed receive – minus
A37	USB0_SS_RX_P	–	AI	USB 0 super-speed receive – plus
E35	USB0_SS_TX_M	–	AO	USB 0 super-speed transmit – minus
E37	USB0_SS_TX_P	–	AO	USB 0 super-speed transmit – plus
C41	USB1_HS_DM	–	AI, AO	USB 1 high-speed data – minus
C39	USB1_HS_DP	–	AI, AO	USB 1 high-speed data – plus
A39	USB1_SS_RX_M	–	AI	USB 1 super-speed receive – minus
A41	USB1_SS_RX_P	–	AI	USB 1 super-speed receive – plus
E39	USB1_SS_TX_M	–	AO	USB 1 super-speed transmit – minus
E41	USB1_SS_TX_P	–	AO	USB 1 super-speed transmit – plus
G41	USB2_HS_DM	–	AI, AO	USB 2 high-speed data – minus
G39	USB2_HS_DP	–	AI, AO	USB 2 high-speed data – plus
AM6	SDC1_CLK	PX_7	DO-NP:pdpukp	Secure digital controller 1 clock for eMMC
AL7	SDC1_CMD	PX_7	B-NP:pdpukp	Secure digital controller 1 command for eMMC

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Table 2-2 Pin descriptions – primary pins (cont.)

Pin no.	Pin name	Pad voltage	Pad type	Functional description
AM10	SDC1_DATA0	PX_7	B-NP:pdpukp	Secure digital controller 1 DATA bit 0 for eMMC
AN7	SDC1_DATA1	PX_7	B-NP:pdpukp	Secure digital controller 1 DATA bit 1 for eMMC
AN9	SDC1_DATA2	PX_7	B-NP:pdpukp	Secure digital controller 1 DATA bit 2 for eMMC
AP8	SDC1_DATA3	PX_7	B-NP:pdpukp	Secure digital controller 1 DATA bit 3 for eMMC
AP10	SDC1_DATA4	PX_7	B-NP:pdpukp	Secure digital controller 1 DATA bit 4 for eMMC
AR7	SDC1_DATA5	PX_7	B-NP:pdpukp	Secure digital controller 1 DATA bit 5 for eMMC
AR9	SDC1_DATA6	PX_7	B-NP:pdpukp	Secure digital controller 1 DATA bit 6 for eMMC
AT8	SDC1_DATA7	PX_7	B-NP:pdpukp	Secure digital controller 1 DATA bit 7 for eMMC
AM8	SDC1_RCLK	PX_7	DI-PD:pdpukp	Secure digital controller 1 return clock for eMMC

Pin descriptions – GPIO pins

GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function–carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

Note Board designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all QCS9075 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

Note Click the following link to download the *QCS9075 + PMM8650AU Pin Assignment and GPIO Configuration Spreadsheet* (80-73417-1A) from the Qualcomm website.

https://docs.qualcomm.com/bundle/80-73417-1A/resource/80-73417-1A

After successfully logging on, the document is downloaded.

Table 2-3 Pin descriptions – GPIO pins

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
BF4	GPIO_0		PX_3	PD:nppukp	Configurable I/O	Y
BE5	GPIO_1		PX_3	PU:nppdkp	Configurable I/O	Y
		PCIE0_CLKREQ_N			PCIe0 clock request	
BF6	GPIO_2		PX_3	PD:nppukp	Configurable I/O	Y
BE7	GPIO_3		PX_3	PU:nppdkp	Configurable I/O	Y
		PCIE1_CLKREQ_N			PCIe1 clock request	
BG7	GPIO_4		PX_3	PD:nppukp	Configurable I/O	Y
BF8	GPIO_5		PX_3	PD:nppukp	Configurable I/O	Y
BD8	GPIO_6		PX_3	PD:nppukp	Configurable I/O	Y
		EMAC0_PTP_AUX_TS_I_0			EMAC0 trigger 0 A for Auxiliary snapshot	
		EMAC0_PTP_PPS_O_0			EMAC0 configurable PPS output 0	
		EMAC1_PTP_AUX_TS_I_0			EMAC1 trigger 0 A for Auxiliary snapshot	
		EMAC1_PTP_PPS_O_0			EMAC1 configurable PPS output 0	
BE9	GPIO_7		PX_3	PD:nppukp	Configurable I/O	Y
		SGMII_PHY_INTR0_N			SGMII0 PHY interrupt	
BG9	GPIO_8		PX_3	PD:nppukp	Configurable I/O	N
		EMAC0_MDC			EMAC0 management interface clock	
BF10	GPIO_9		PX_3	PD:nppukp	Configurable I/O	N
		EMAC0_MDIO			EMAC0 management interface I/O	
		GP_PDM_MIRA[2]			General-purpose PDM output 2 A	
BD2	GPIO_10		PX_3	PD:nppukp	Configurable I/O	Y
		USB2PHY_AC_EN0			USB AC coupling control for USB0 port	
		EMAC0_PTP_AUX_TS_I_1			EMAC0 trigger 1 A for Auxiliary snapshot	
		EMAC0_PTP_PPS_O_1			EMAC0 configurable PPS output 1	

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		EMAC1_PTP_AUX_TS_I_1			EMAC1 trigger 1 A for Auxiliary snapshot	
		EMAC1_PTP_PPS_O_1			EMAC1 configurable PPS output 1	
		GP_PDM_MIRB[2]			General-purpose PDM output 2 B	
		BOOT_CONFIG[12]			Boot configuration bit 12	
BD4	GPIO_11		PX_3	PD:nppukp	Configurable I/O	Y
		USB2PHY_AC_EN1			USB AC coupling control for USB 1 port	
		EMAC0_PTP_AUX_TS_I_2			EMAC0 trigger 2 A for Auxiliary snapshot	
		EMAC0_PTP_PPS_O_2			EMAC0 configurable PPS output 2	
		EMAC1_PTP_AUX_TS_I_2			EMAC1 trigger 2 A for Auxiliary snapshot	
		EMAC1_PTP_PPS_O_2			EMAC1 configurable PPS output 2	
		GP_PDM_MIRA[1]			General-purpose PDM output 1 A	
		BOOT_CONFIG[13]			Boot configuration bit 13	
BE3	GPIO_12		PX_3	PD:nppukp	Configurable I/O	Y
		USB2PHY_AC_EN2			USB AC coupling control for USB 2 port	
		EMAC0_PTP_AUX_TS_I_3			EMAC0 trigger 3 A for Auxiliary snapshot	
		EMAC0_PTP_PPS_O_3			EMAC0 configurable PPS output 3	
		EMAC1_PTP_AUX_TS_I_3			EMAC1 trigger 3 A for Auxiliary snapshot	
		EMAC1_PTP_PPS_O_3			EMAC1 configurable PPS output 3	
		EMAC0_MCG_PST_TRIG_LW[0]			EMAC0 trigger input 0 for Media clock generation	
		GP_PDM_MIRB[1]			General-purpose PDM output 1 B	
		BOOT_CONFIG[14]			Boot configuration bit 14	
J1	GPIO_13		PX_3	PD:nppukp	Configurable I/O	N

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		QUP3_SE0_L0			QUP3 SE0 lane 0: UART_CTS/HS-UART_CTS/I2C_SDA/SPI-M_MISO/ QSPI_MISO	
		EMAC0_MCG_PST_TRIG_LW[1]			EMAC0 trigger input 1 for Media clock generation	
J3	GPIO_14		PX_3	PD:nppukp	Configurable I/O	N
		QUP3_SE0_L1			QUP3 SE0 lane 1: UART_RFR/HS-UART_RFR/ /I2C_SCL/SPI-M_MOSI/QSPI_MOSI	
		EMAC0_MCG_PST_TRIG_LW[2]			EMAC0 trigger input 2 for Media clock generation	
J5	GPIO_15		PX_3	PD:nppukp	Configurable I/O	N
		QUP3_SE0_L2			QUP3 SE0 lane 2: UART_TX/HS-UART_TX/SPI-M_SCLK/QSPI_SCLK	
		EMAC0_MCG_PST_TRIG_LW[3]			EMAC0 trigger input 3 for Media clock generation	
K2	GPIO_16		PX_3	PD:nppukp	Configurable I/O	Y
		QUP3_SE0_L3			QUP3 SE0 lane 3: UART_RX/HS-UART_RX/SPI-M_CS0/QSPI_CS	
		EMAC1_MCG_PST_TRIG_LW[3]			EMAC1 trigger input 0 for Media clock generation	
K4	GPIO_17		PX_3	PD:nppukp	Configurable I/O	N
		QUP3_SE0_L4			QUP3 SE0 lane 4: SPI-M_CS1/ QSPI_IO2	
		EMAC1_MCG_PST_TRIG_LW[1]			EMAC1 trigger input 1 for Media clock generation	
L1	GPIO_18		PX_3	PD:nppukp	Configurable I/O	N
		QUP3_SE0_L5			QUP3 SE0 lane 5: SPI-M_CS2/ QSPI_IO3	
		EMAC1_MCG_PST_TRIG_LW[2]			EMAC1 trigger input 2 for Media clock generation	
L3	GPIO_19		PX_3	PD:nppukp	Configurable I/O	Y

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		QUP3_SE0_L6			QUP3 SE0 lane 6: QSPI_INT	
		EMAC1_MCG_PST_TRIG_LW[3]			EMAC1 trigger input 3 for Media clock generation	
BG21	GPIO_20		PX_3	PD:nppukp	Configurable I/O	Y
		QUP0_SE0_L0			QUP0 SE0 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO	
		EMAC1_MDC			EMAC1 management interface clock	
BG19	GPIO_21		PX_3	PD:nppukp	Configurable I/O	N
		QUP0_SE0_L1			QUP0 SE0 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI	
		EMAC1_MDIO			EMAC1 management interface I/O	
BE21	GPIO_22		PX_3	PD:nppukp	Configurable I/O	N
		QUP0_SE0_L2			QUP0 SE0 lane 2: UART_TX/SPI-M_SCLK	
BF20	GPIO_23		PX_3	PD:nppukp	Configurable I/O	Y
		QUP0_SE0_L3			QUP0 SE0 lane 3: UART_RX/SPI-M_CS0	
BD20	GPIO_24		PX_3	PD:nppukp	Configurable I/O	Y
		QUP0_SE1_L0			QUP0 SE1 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO	
BE19	GPIO_25		PX_3	PD:nppukp	Configurable I/O	N
		QUP0_SE1_L1			QUP0 SE1 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI	
BF18	GPIO_26		PX_3	PD:nppukp	Configurable I/O	Y
		SGMII_PHY_INTR1_N			SGMII1 PHY interrupt	
		QUP0_SE1_L2			QUP0 SE1 lane 2: UART_TX/SPI-M_SCLK	
BD18	GPIO_27		PX_3	PD:nppukp	Configurable I/O	Y
		QUP0_SE1_L3			QUP0 SE1 lane 3: UART_RX/SPI-M_CS0	

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
BG15	GPIO_28		PX_3	PD:nppukp	Configurable I/O	Y
		QUP0_SE3_L0			QUP0 SE3 lane 0: UART_CTS/HS-UART_CTS/I2C_SDA/SPI-M_MISO	
BE17	GPIO_29		PX_3	PD:nppukp	Configurable I/O	Y
		QUP0_SE3_L1			QUP0 SE3 lane 1: UART_RFR/HS-UART_RFR/I2C_SCL/SPI-M_MOSI	
BF16	GPIO_30		PX_3	PD:nppukp	Configurable I/O	Y
		QUP0_SE3_L2			QUP0 SE3 lane 2: UART_TX/HS-UART_TX/SPI-M_SCLK	
BD16	GPIO_31		PX_3	PD:nppukp	Configurable I/O	Y
		QUP0_SE3_L3			QUP0 SE3 lane 3: UART_RX/HS-UART_RX/SPI-M_CS0	
BG13	GPIO_32		PX_3	PD:nppukp	Configurable I/O	Y
		QUP0_SE4_L0			QUP0 SE4 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO/SPI-S_MISO	
BE15	GPIO_33		PX_3	PD:nppukp	Configurable I/O	N
		QUP0_SE4_L1			QUP0 SE4 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI/SPI-S_MOSI	
		GCC_GP4_CLK_MIRA			General-purpose Clock 4 A	
BF14	GPIO_34		PX_3	PD:nppukp	Configurable I/O	N
		QUP0_SE4_L2			QUP0 SE4 lane 2: UART_TX/SPI-M_SCLK/SPI-S_SCLK	
		GCC_GP5_CLK_MIRA			General-purpose Clock 5 A	
BE13	GPIO_35		PX_3	PD:nppukp	Configurable I/O	Y
		QUP0_SE4_L3			QUP0 SE4 lane 3: UART_RX/SPI-M_CS0/SPI-M_CS	
		GP_MN			General-purpose M/N:D counter output	
BF12	GPIO_36		PX_3	PD:nppukp	Configurable I/O	Y

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		QUP0_SE2_L0			QUP0 SE2 lane 0: UART_CTS/HS-UART_CTS/I2C_SDA/SPI-M_MISO	
		QUP0_SE5_L0			QUP0 SE5 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO/SPI-S_MISO	
BD12	GPIO_37		PX_3	PD:nppukp	Configurable I/O	N
		QUP0_SE2_L1			QUP0 SE2 lane 1: UART_RFR/HS-UART_RFR/I2C_SCL/SPI-M_MOSI	
		QUP0_SE5_L1			QUP0 SE5 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI/SPI-S_MOSI	
BE11	GPIO_38		PX_3	PD:nppukp	Configurable I/O	N
		QUP0_SE5_L2			QUP0 SE5 lane 2: UART_TX/SPI-M_SCLK/SPI-S_SCLK	
		QUP0_SE2_L2			QUP0 SE2 lane 2: UART_TX/HS-UART_TX/SPI-M_SCLK	
		BOOT_CONFIG[1]			Boot configuration bit 1	
BD10	GPIO_39		PX_3	PD:nppukp	Configurable I/O	Y
		QUP0_SE5_L3			QUP0 SE5 lane 3: UART_RX/SPI-M_CS0/SPI-S_CS	
		QUP0_SE2_L3			QUP0 SE2 lane 3: UART_RX/HS-UART_RX/SPI-M_CS0	
BD30	GPIO_40		PX_3	PD:nppukp	Configurable I/O	Y
		QUP1_SE0_L0			QUP1 SE0 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO	
		QUP1_SE1_L2			QUP1 SE1 lane 2: UART_TX/SPI-M_SCLK	
BE27	GPIO_41		PX_3	PD:nppukp	Configurable I/O	Y
		QUP1_SE0_L1			QUP1 SE0 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI	
		QUP1_SE1_L3			QUP1 SE1 lane 3: UART_RX/SPI-M_CS0	
BD38	GPIO_42		PX_3	PD:nppukp	Configurable I/O	Y

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		QUP1_SE1_L0			QUP1 SE1 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO	
		QUP1_SE0_L2			QUP1 SE0 lane 2: UART_TX/SPI-M_SCLK	
		GCC_GP5_CLK_MIRB			General-purpose Clock 5 B	
BE37	GPIO_43		PX_3	PD:nppukp	Configurable I/O	Y
		QUP1_SE1_L1			QUP1 SE1 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI	
		QUP1_SE0_L3			QUP1 SE0 lane 3: UART_RX/SPI-M_CS0	
BD36	GPIO_44		PX_3	PD:nppukp	Configurable I/O	N
		QUP1_SE2_L2			QUP1 SE2 lane 2: UART_TX/HS-UART_TX/SPI-M_SCLK	
		QUP1_SE3_L0			QUP1 SE3 lane 0: UART_CTS/HS-UART_CTS/I2C_SDA/SPI-M_MISO	
BC37	GPIO_45		PX_3	PD:nppukp	Configurable I/O	Y
		QUP1_SE2_L3			QUP1 SE2 lane 3: UART_RX/HS-UART_RX/SPI-M_CS0	
		QUP1_SE3_L1			QUP1 SE3 lane 1: UART_RFR/HS-UART_RFR/I2C_SCL/SPI-M_MOSI	
BE35	GPIO_46		PX_3	PD:nppukp	Configurable I/O	N
		QUP1_SE3_L2			QUP1 SE3 lane 2: UART_TX/HS-UART_TX/SPI-M_SCLK	
		QUP1_SE2_L0			QUP1 SE2 lane 0: UART_CTS/HS-UART_CTS/I2C_SDA/SPI-M_MISO	
BD34	GPIO_47		PX_3	PD:nppukp	Configurable I/O	Y
		QUP1_SE3_L3			QUP1 SE3 lane 3: UART_RX/HS-UART_RX/SPI-M_CS0	
		QUP1_SE2_L1			QUP1 SE2 lane 1: UART_RFR/HS-UART_RFR/I2C_SCL/SPI-M_MOSI	
BE29	GPIO_48		PX_3	PD:nppukp	Configurable I/O	Y

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		QUP1_SE4_L0			QUP1 SE4 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO/SPI-S_MISO	
		BOOT_CONFIG[0]			Boot configuration bit 0	
BD32	GPIO_49		PX_3	PD:nppukp	Configurable I/O	N
		QUP1_SE4_L1			QUP1 SE4 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI/SPI-S_MOSI	
BF26	GPIO_50		PX_3	PD:nppukp	Configurable I/O	N
		QUP1_SE4_L2			QUP1 SE4 lane 2: UART_TX/SPI-M_SCLK/SPI-S_SCLK	
		CCI_ASYNC_IN4			Camera control interface async 4	
		FORCED_USB_BOOT			Boot strap to enter USB0 emergency download mode. See *QCS9075M Technical Reference Manual* (80-73418-5) (to be released) for details.	
BD26	GPIO_51		PX_3	PD:nppukp	Configurable I/O	Y
		QUP1_SE4_L3			QUP1 SE4 lane 3: UART_RX/SPI-M_CS0/SPI-S_CS	
		GCC_GP1_CLK_MIRB			General-purpose Clock 1 B	
BE25	GPIO_52		PX_3	PD:nppukp	Configurable I/O	Y
		QUP1_SE5_L0			QUP1 SE5 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO/SPI-S_MISO	
		CCI_TIMER4			Camera 4 control interface timer	
		CCI_I2C_SDA1			Camera 1 I^2C Data	
		GCC_GP2_CLK_MIRB			General-purpose Clock 2 B	
BG25	GPIO_53		PX_3	PD:nppukp	Configurable I/O	N
		QUP1_SE5_L1			QUP1 SE5 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI/SPI-S_MOSI	
		CCI_TIMER5			Camera 5 control interface timer	
		CCI_I2C_SCL1			Camera 1 I2C clock	

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		GCC_GP3_CLK_MIRB			General-purpose Clock 3 B	
BF24	GPIO_54		PX_3	PD:nppukp	Configurable I/O	N
		QUP1_SE5_L2			QUP1 SE5 lane 2: UART_TX/SPI-M_SCLK/SPI-S_SCLK	
		CCI_TIMER6			Camera 6 control interface timer	
		CCI_I2C_SDA3			Camera 3 I2C Data	
BD24	GPIO_55		PX_3	PD:nppukp	Configurable I/O	Y
		QUP1_SE5_L3			QUP1 SE5 lane 3: UART_RX/SPI-M_CS0/SPI-M_CS	
		CCI_TIMER7			Camera 7 control interface timer	
		CCI_I2C_SCL3			Camera 3 I2C clock	
		GCC_GP4_CLK_MIRB			General-purpose Clock 4 B	
BE23	GPIO_56		PX_3	PD:nppukp	Configurable I/O	Y
		QUP1_SE6_L0			QUP1 SE6 lane 0: UART_CTS/ I2C_SDA	
		QUP1_SE6_L2			QUP1 SE6 lane 2: UART_TX	
		CCI_TIMER8			Camera 8 control interface timer	
		CCI_I2C_SDA5			Camera 5 I2C Data	
BF22	GPIO_57		PX_3	PD:nppukp	Configurable I/O	Y
		QUP1_SE6_L1			QUP1 SE6 lane 1: UART_RFR/ I2C_SCL	
		QUP1_SE6_L3			QUP1 SE6 lane 3: UART_RX	
		CCI_TIMER9			Camera 9 control interface timer	
		CCI_I2C_SCL5			Camera 5 I2C Clock	
BB10	GPIO_58		PX_3	PD:nppukp	Configurable I/O	Y
		CCI_I2C_SDA7			Camera 7 I2C Data	
		BOOT_CONFIG[11]			Boot configuration bit 11	
BC11	GPIO_59		PX_3	PD:nppukp	Configurable I/O	Y

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		CCI_I2C_SCL7			Camera 7 I2C clock	
BB12	GPIO_60		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA0			Camera 0 I2C Data	
BC13	GPIO_61		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL0			Camera 0 I2C clock	
BB14	GPIO_62		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA2			Camera 2 I2C Data	
AY14	GPIO_63		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL2			Camera 2 I2C clock	
BA15	GPIO_64		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA4			Camera 4 I2C Data	
BC15	GPIO_65		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL4			Camera 4 I2C clock	
BB16	GPIO_66		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SDA6			Camera 6 I2C Data	
		CCI_ASYNC_IN5			Camera control interface async 5	
AY16	GPIO_67		PX_3	PD:nppukp	Configurable I/O	N
		CCI_I2C_SCL6			Camera 6 I2C clock	
BC33	GPIO_68		PX_3	PD:nppukp	Configurable I/O	N
		CCI_TIMER0			Camera 0 control interface timer	
		CCI_ASYNC_IN0			Camera control interface async 0	
BA35	GPIO_69		PX_3	PD:nppukp	Configurable I/O	N
		CCI_TIMER1			Camera 1 control interface timer	
		CCI_ASYNC_IN1			Camera control interface async 1	
AY36	GPIO_70		PX_3	PD:nppukp	Configurable I/O	N
		CCI_TIMER2			Camera 2 control interface timer	
		CCI_ASYNC_IN2			Camera control interface async 2	

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
BB34	GPIO_71		PX_3	PD:nppukp	Configurable I/O	N
		CCI_TIMER3			Camera 3 control interface timer	
		CCI_ASYNC_IN3			Camera control interface async 3	
BB32	GPIO_72		PX_3	PD:nppukp	Configurable I/O	Y
		CAM_MCLK0			Camera 0 MCLK	
BA33	GPIO_73		PX_3	PD:nppukp	Configurable I/O	Y
		CAM_MCLK1			Camera 1 MCLK	
AY34	GPIO_74		PX_3	PD:nppukp	Configurable I/O	Y
		CAM_MCLK2			Camera 2 MCLK	
BA31	GPIO_75		PX_3	PD:nppukp	Configurable I/O	Y
		CAM_MCLK3			Camera 3 MCLK	
BC29	GPIO_76		PX_3	PD:nppukp	Configurable I/O	Y
BB30	GPIO_77		PX_3	PD:nppukp	Configurable I/O	Y
AY32	GPIO_78		PX_3	PD:nppukp	Configurable I/O	Y
AY30	GPIO_79		PX_3	PD:nppukp	Configurable I/O	Y
BC27	GPIO_80		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE0_L0			QUP2 SE0 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO	
		GP_PDM_MIRA[0]			General-purpose PDM output 0 A	
BA27	GPIO_81		PX_3	PD:nppukp	Configurable I/O	N
		QUP2_SE0_L1			QUP2 SE0 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI	
		GP_PDM_MIRB[0]			General-purpose PDM output 0 B	
AY26	GPIO_82		PX_3	PD:nppukp	Configurable I/O	N
		QUP2_SE0_L2			QUP2 SE0 lane 2: UART_TX/SPI-M_SCLK	
		MDP_VSYNC_S			MDP vertical sync	
		GCC_GP1_CLK_MIRA			General-purpose Clock 1 A	

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
BB26	GPIO_83		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE0_L3			QUP2 SE0 lane 3: UART_RX/SPI-M_CS0	
		MDP_VSYNC_E			MDP vertical sync – external	
		GCC_GP2_CLK_MIRA			General-purpose Clock 2 A	
BC25	GPIO_84		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE1_L0			QUP2 SE1 lane 0: UART_CTS/I2C_SDA/SPI-M_MISO	
		QUP2_SE5_L2			QUP2 SE5 lane 2: UART_TX/SPI-M_SCLK/SPI-S_SCLK	
		MDP_VSYNC_P			MDP vertical sync – Primary	
		GCC_GP3_CLK_MIRA			General-purpose Clock 3 A	
BA25	GPIO_85		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE1_L1			QUP2 SE1 lane 1: UART_RFR/I2C_SCL/SPI-M_MOSI	
		QUP2_SE5_L3			QUP2 SE5 lane 3: UART_RX/SPI-M_CS0/SPI-M_CS	
AY24	GPIO_86		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE2_L0			QUP2 SE2 lane 0: UART_CTS/HS-UART_CTS/I2C_SDA/SPI-M_MISO	
BC23	GPIO_87		PX_3	PD:nppukp	Configurable I/O	N
		QUP2_SE2_L1			QUP2 SE2 lane 1: UART_RFR/HS-UART_RFR/I2C_SCL/SPI-M_MOSI	
AY22	GPIO_88		PX_3	PD:nppukp	Configurable I/O	N
		QUP2_SE2_L2			QUP2 SE2 lane 2: UART_TX/HS-UART_TX/SPI-M_SCLK	
BA23	GPIO_89		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE2_L3			QUP2 SE2 lane 3: UART_RX/HS-UART_RX/SPI-M_CS0	
BB22	GPIO_90		PX_3	PD:nppukp	Configurable I/O	N

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		QUP2_SE2_L4			QUP2 SE2 lane 4: SPI-M_CS1	
BC21	GPIO_91		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE3_L0			QUP2 SE3 lane 0: UART_CTS/HS-UART_CTS/I2C_SDA/SPI-M_MISO	
BA21	GPIO_92		PX_3	PD:nppukp	Configurable I/O	N
		QUP2_SE3_L1			QUP2 SE3 lane 1: UART_RFR/HS-UART_RFR/I2C_SCL/SPI-M_MOSI	
AY20	GPIO_93		PX_3	PD:nppukp	Configurable I/O	N
		QUP2_SE3_L2			QUP2 SE3 lane 2: UART_TX/HS-UART_TX/SPI-M_SCLK	
BB20	GPIO_94		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE3_L3			QUP2 SE3 lane 3: UART_RX/HS-UART_RX/SPI-M_CS0	
BC19	GPIO_95		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE4_L0			QUP2 SE4 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO/SPI-S_MISO	
		QUP2_SE6_L2			QUP2 SE6 lane 2: UART_TX/SPI-M_SCLK	
BA19	GPIO_96		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE4_L1			QUP2 SE4 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI/SPI-S_MOSI	
		QUP2_SE6_L3			QUP2 SE6 lane 3: UART_RX/SPI-M_CS0	
AY18	GPIO_97		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE6_L0			QUP2 SE6 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO	
		QUP2_SE4_L2			QUP2 SE4 lane 2: UART_TX/SPI-M_SCLK/SPI-S_SCLK	
BB18	GPIO_98		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE6_L1			QUP2 SE6 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI	

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		QUP2_SE4_L3			QUP2 SE4 lane 3: UART_RX/SPI-M_CS0/SPI-M_CS	
BA17	GPIO_99		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE5_L0			QUP2 SE5 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO/SPI-S_MISO	
		QUP2_SE1_L2			QUP2 SE1 lane 2: UART_TX/SPI-M_SCLK	
BC17	GPIO_100		PX_3	PD:nppukp	Configurable I/O	Y
		QUP2_SE5_L1			QUP2 SE5 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI/SPI-S_MOSI	
		QUP2_SE1_L3			QUP2 SE1 lane 3: UART_RX/SPI-M_CS0	
BA37	GPIO_101		PX_3	PD:nppukp	Configurable I/O	N
		EDP0_HOT_PLUG_DETECT			Embedded DisplayPort 0 hot plug detect	
BB38	GPIO_102		PX_3	PD:nppukp	Configurable I/O	N
		EDP1_HOT_PLUG_DETECT			Embedded DisplayPort 1 hot plug detect	
AY40	GPIO_103		PX_3	PD:nppukp	Configurable I/O	N
		EDP3_HOT_PLUG_DETECT			Embedded DisplayPort 3 hot plug detect	
AY38	GPIO_104		PX_3	PD:nppukp	Configurable I/O	N
		EDP2_HOT_PLUG_DETECT			Embedded DisplayPort 2 hot plug detect	
AP78	GPIO_105		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S_MCLK0			MI2S master clock 0	
		BOOT_CONFIG[2]			Boot configuration bit 2	
AP80	GPIO_106		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S1_SCK_OR_HS3_MI2S_SCK			MI2S 1 clock or high-speed 3 MI2S clock	

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		BOOT_CONFIG[3]			Boot configuration bit 3	
AR71	GPIO_107		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S1_WS_OR_HS3_MI2S_WS			MI2S 1 word select or high-speed 3 MI2S word select and synchronization	
		RESERVED			Reserved boot configuration pin. See *QCS9075 Technical Reference Manual* (80-73418-5) (to be released) for details.	
AR73	GPIO_108		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S1_DATA0_OR_HS3_MI2S_DATA 0			MI2S 1 serial data channel 0 or high speed 3 MI2S serial data channel 0	
AR75	GPIO_109		PX_3	PD:nppukp	Configurable I/O	Y
		MI2S1_DATA1_OR_HS3_MI2S_DATA 1			MI2S 1 serial data channel 1 or high speed 3 MI2S serial data channel 1	
AR77	GPIO_110		PX_3	PD:nppukp	Configurable I/O	N
		MI2S2_SCK_OR_HS4_MI2S_SCK			MI2S 2 clock or High-speed 4 MI2S clock	
		BOOT_CONFIG[4]			Boot configuration bit 4	
AR81	GPIO_111		PX_3	PD:nppukp	Configurable I/O	N
		MI2S2_WS_OR_HS4_MI2S_WS			MI2S 2 serial data word select or high-speed 4 MI2S 2 serial data word select and synchronization	
AT70	GPIO_112		PX_3	PD:nppukp	Configurable I/O	N
		MI2S2_DATA0_OR_HS4_MI2S_DATA 0			MI2S 2 serial data channel 0 or high speed 4 MI2S serial data channel 0	
AT72	GPIO_113		PX_3	PD:nppukp	Configurable I/O	N
		MI2S2_DATA1_OR_HS4_MI2S_DATA 1			MI2S 2 serial data channel 1 or high speed 4 MI2S serial data channel 1	
		AUDIO_REF_CLK			Audio reference clock	
AT76	GPIO_114		PX_3	PD:nppukp	Configurable I/O	N

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		HS_I2S0_SCK			High-speed 0 MI2S clock	
AT78	GPIO_115		PX_3	PD:nppukp	Configurable I/O	N
		HS_I2S0_WS			High-speed 0 MI2S word select	
AU71	GPIO_116		PX_3	PD:nppukp	Configurable I/O	N
		HS_I2S0_DATA0			High-speed 0 MI2S data 0	
AU73	GPIO_117		PX_3	PD:nppukp	Configurable I/O	N
		HS_I2S0_DATA1			High-speed 0 MI2S data 1	
		MI2S_MCLK1			MI2S master clock 1	
AU75	GPIO_118		PX_3	PD:nppukp	Configurable I/O	N
		HS_I2S1_WS			High-speed 1 MI2S word select	
AU77	GPIO_119		PX_3	PD:nppukp	Configurable I/O	N
		HS_I2S1_SCK			High-speed 1 MI2S clock	
AV70	GPIO_120		PX_3	PD:nppukp	Configurable I/O	N
		HS_I2S1_DATA0			High-speed 1 MI2S data 0	
AV72	GPIO_121		PX_3	PD:nppukp	Configurable I/O	N
		HS_I2S1_DATA1			High-speed 1 MI2S data 1	
AW71	GPIO_122		PX_3	PD:nppukp	Configurable I/O	N
		HS_I2S2_SCK			High-speed 2 MI2S clock	
AW73	GPIO_123		PX_3	PD:nppukp	Configurable I/O	N
		HS_I2S2_WS			High-speed 2 MI2S word select	
AW75	GPIO_124		PX_3	PD:nppukp	Configurable I/O	N
		HS_I2S2_DATA0			High-speed 2 MI2S data 0	
AW77	GPIO_125		PX_3	PD:nppukp	Configurable I/O	N
		HS_I2S2_DATA1			High-speed 2 MI2S data 1	
AJ77	GPIO_126		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_0			See Table 2-5 for details	
AK72	GPIO_127		PX_3	PD:nppukp	Configurable I/O	N

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
		LPASS_1			See Table 2-5 for details	
AK76	GPIO_128		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_2			See Table 2-5 for details	
AK78	GPIO_129		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_3			See Table 2-5 for details	
AK80	GPIO_130		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_4			See Table 2-5 for details	
AL71	GPIO_131		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_5			See Table 2-5 for details	
AL73	GPIO_132		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_6			See Table 2-5 for details	
AL75	GPIO_133		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_7			See Table 2-5 for details	
AL77	GPIO_134		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_8			See Table 2-5 for details	
AL81	GPIO_135		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_9			See Table 2-5 for details	
AM70	GPIO_136		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_10			See Table 2-5 for details	
AM72	GPIO_137		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_11			See Table 2-5 for details	
AM76	GPIO_138		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_15			See Table 2-5 for details	
AM78	GPIO_139		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_16			See Table 2-5 for details	
AM80	GPIO_140		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_14			See Table 2-5 for details	

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Table 2-3 Pin descriptions – GPIO pins (cont.)

Pin no.	Pin name and/or function	Alternate function	Pad characteristics		Functional description	Wakeup function
			Voltage	Type		
AN71	GPIO_141		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_12			See Table 2-5 for details	
AN73	GPIO_142		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_13			See Table 2-5 for details	
AN75	GPIO_143		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_17			See Table 2-5 for details	
AN77	GPIO_144		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_18			See Table 2-5 for details	
AN81	GPIO_145		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_19			See Table 2-5 for details	
AP70	GPIO_146		PX_3	PD:nppukp	Configurable I/O	Y
		LPASS_20			See Table 2-5 for details	
AP72	GPIO_147		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_21			See Table 2-5 for details	
AP76	GPIO_148		PX_3	PD:nppukp	Configurable I/O	N
		LPASS_22			See Table 2-5 for details	

Table 2-4 Pin descriptions – RTSS I/O

Pin number	RTSS I/O	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup function
P4	RTSS_IO_0		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE0_L0			RTSS QUP0 SE0 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO/SPI-S_MISO	
P2	RTSS_IO_1		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE0_L1			RTSS QUP0 SE0 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI/SPI-S_MOSI	
R3	RTSS_IO_2		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y

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Table 2-4 Pin descriptions – RTSS I/O (cont.)

Pin number	RTSS I/O	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup function
		RTSS_QUP0_SE1_L0			RTSS QUP0 SE1 lane 0: UART_CTS/ I2C_SDA/SPI-M_MISO/SPI-S_MISO	
R5	RTSS_IO_3		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE1_L1			RTSS QUP0 SE1 lane 1: UART_RFR/ I2C_SCL/SPI-M_MOSI/SPI-S_MOSI	
T2	RTSS_IO_4		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE1_L2			RTSS QUP0 SE1 lane 2: UART_TX/SPI-M_SCLK/SPI-S_SCLK	
		RTSS_QUP0_SE3_L2			RTSS QUP0 SE3 lane 2: UART_TX/HS UART_TX/SPI-M_SCLK	
T4	RTSS_IO_5		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE1_L3			RTSS QUP0 SE1 lane 3: UART_RX/SPI-M_CS0/SPI-S_CS	
		RTSS_QUP0_SE3_L3			RTSS QUP0 SE3 lane 3: UART_RX/HS-UART_RX/SPI-M_CS0	
U1	RTSS_IO_6		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE2_L2			RTSS QUP0 SE2 lane 2: UART_TX/HS UART_TX/SPI-M_SCLK	
		RTSS_QUP0_SE0_L2			RTSS QUP0 SE0 lane 2: UART_TX/SPI-M_SCLK/SPI-S_SCLK	
		RTSS_BOOT_CONFIG[13]			RTSS Boot configuration bit 13	
U3	RTSS_IO_7		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_QUP0_SE2_L3			RTSS QUP0 SE2 lane 3: UART_RX/HS-UART_RX/SPI-M_CS0	
		RTSS_QUP0_SE0_L3			RTSS QUP0 SE0 lane 3: UART_RX/SPI-M_CS0/SPI-S_CS	
		RTSS_BOOT_CONFIG[14]			RTSS Boot configuration bit 14	
U5	RTSS_IO_8		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE3_L0			RTSS QUP0 SE3 lane 0: UART_CTS/HS-UART_CTS/I2C_SDA/SPI-M_MISO	
		RTSS_QUP0_SE2_L0			RTSS QUP0 SE2 lane 0: UART_CTS/HS-UART_CTS/I2C_SDA/SPI-M_MISO	

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Table 2-4 Pin descriptions – RTSS I/O (cont.)

Pin number	RTSS I/O	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup function
V2	RTSS_IO_9		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE3_L1			RTSS QUP0 SE3 lane 1: UART_RFR/HS-UART_RFR/I2C_SCL/ SPI-M_MOSI	
		RTSS_QUP0_SE2_L1			RTSS QUP0 SE2 lane 1: UART_RFR/HS-UART_RFR /I2C_SCL/SPI-M_MOSI	
V4	RTSS_IO_10		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_QUP0_SE4_L0			RTSS QUP0 SE4 lane 0: UART_CTS/ I2C_SDA/ SPI-M_MISO	
W3	RTSS_IO_11		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE4_L1			RTSS QUP0 SE4 lane 1: UART_RFR/ / I2C_SCL/ SPI-M_MOSI	
W5	RTSS_IO_12		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE4_L2			RTSS QUP0 SE4 lane 2: UART_TX/SPI-M_SCLK	
Y2	RTSS_IO_13		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE4_L3			RTSS QUP0 SE4 lane 3: UART_RX/SPI-M_CS0	
Y4	RTSS_IO_14		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_QUP0_SE4_L4			RTSS QUP0 SE4 lane 4: SPI-M_CS1	
		RTSS_BOOT_CONFIG[6]			RTSS Boot configuration bit 6	
AA5	RTSS_IO_15		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RESERVED (ES1 only)			Reserved boot configuration pin. See *QCS9075 Technical Reference Manual* (80-73418-5) (to be released) for details.	
		RTSS_FORCED_USB_BOOT (ES2 and later)			Bootstrap to enter USB0 emergency download mode for RTSS domain. See *QCS9075 Technical Reference Manual* (80-73418-5) (to be released) for details.	
AA3	RTSS_IO_16		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_RGMII_VOL_SEL			Voltage selection pin for RTSS RGMII interface	
AA1	RTSS_IO_17		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y

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Table 2-4 Pin descriptions – RTSS I/O (cont.)

Pin number	RTSS I/O	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup function
		RTSS_BOOT_CONFIG[11]			RTSS Boot configuration bit 11	
T6	RTSS_IO_18		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_BOOT_CONFIG[12]			RTSS Boot configuration bit 12	
AV6	RTSS_IO_19		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_ERR1			RTSS error 1 (default output LOW)	
AU5	RTSS_IO_20		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_ERR2			RTSS SS error 1 (default output HIGH)	
BB8	RTSS_IO_21		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_EMAC0_PHY_INTR_N			RTSS Ethernet interrupt 0	
BB6	RTSS_IO_22		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_MDC			RTSS RGMII 0 management interface clock	
BC7	RTSS_IO_23		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_MDIO			RTSS RGMII 0 management interface clock	
BA3	RTSS_IO_24		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_RXC			RTSS RGMII 0 receive clock signal	
AY4	RTSS_IO_25		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_RX_CTL			RTSS RGMII 0 receive control	
AY2	RTSS_IO_26		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_RXD0			RTSS RGMII 0 receive data 0	
AW5	RTSS_IO_27		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_RXD1			RTSS RGMII 0 receive data 1	
AW3	RTSS_IO_28		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_RXD2			RTSS RGMII 0 receive data 2	
AW1	RTSS_IO_29		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_RXD3			RTSS RGMII 0 receive data 3	
BC1	RTSS_IO_30		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_TXC			RTSS RGMII 0 transmit clock signal	

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Table 2-4 Pin descriptions – RTSS I/O (cont.)

Pin number	RTSS I/O	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup function
BC3	RTSS_IO_31		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_TX_CTL			RTSS RGMII 0 transmit control	
BC5	RTSS_IO_32		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_TXD0			RTSS RGMII 0 transmit data 0	
BB4	RTSS_IO_33		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_TXD1			RTSS RGMII 0 transmit data 1	
BA5	RTSS_IO_34		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_TXD2			RTSS RGMII 0 transmit data 2	
BB2	RTSS_IO_35		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_RGMII0_TXD3			RTSS RGMII 0 transmit data 3	
BA7	RTSS_IO_36		RTSS_PX_8	PD:nppukp	RTSS domain configurable I/O	N
AB2	RTSS_IO_37		RTSS_PX_3	PU:nppdkp	RTSS domain configurable I/O	N
		RTSS_CAN0_TX			RTSS CAN 0 transmit	
		RTSS_BOOT_CONFIG[0]			RTSS Boot configuration bit 0	
AB4	RTSS_IO_38		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_CAN0_RX			RTSS CAN 0 receive	
		RTSS_CC_GP2_CLK_MIRA			RTSS Global general-purpose clock 2 A	
AD4	RTSS_IO_39		RTSS_PX_3	PU:nppdkp	RTSS domain configurable I/O	N
		RTSS_CAN1_TX			RTSS CAN 1 transmit	
		RTSS_BOOT_CONFIG[1]			RTSS Boot configuration bit 1	
AC3	RTSS_IO_40		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_CAN1_RX			RTSS CAN 1 receive	
		RTSS_CC_GP2_CLK_MIRB			RTSS Global general-purpose clock 2 B	
AD2	RTSS_IO_41		RTSS_PX_3	PU:nppdkp	RTSS domain configurable I/O	N
		RTSS_CAN2_TX			RTSS CAN 2 transmit	
AE5	RTSS_IO_42		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_CAN2_RX			RTSS CAN 2 receive	

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Table 2-4 Pin descriptions – RTSS I/O (cont.)

Pin number	RTSS I/O	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup function
		RTSS_CC_GP3_CLK_MIRA			RTSS Global general-purpose clock 3 A	
AE3	RTSS_IO_43		RTSS_PX_3	PU:nppdkp	RTSS domain configurable I/O	N
		RTSS_CAN3_TX			RTSS CAN 3 transmit	
		RTSS_BOOT_CONFIG[2]			RTSS Boot configuration bit 2	
AE1	RTSS_IO_44		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_CAN3_RX			RTSS CAN 3 receive	
		RTSS_CC_GP3_CLK_MIRB			RTSS Global general-purpose clock 3 B	
AF4	RTSS_IO_45		RTSS_PX_3	PU:nppdkp	RTSS domain configurable I/O	N
		RTSS_CAN4_TX			RTSS CAN 4 transmit	
		RTSS_BOOT_CONFIG[3]			RTSS Boot configuration bit 3	
AF2	RTSS_IO_46		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_CAN4_RX			RTSS CAN 4 receive	
		RTSS_CC_GP4_CLK_MIRA			RTSS Global general-purpose clock 4 A	
AG5	RTSS_IO_47		RTSS_PX_3	PU:nppdkp	RTSS domain configurable I/O	N
		RTSS_CAN5_TX			RTSS CAN 5 transmit	
AG3	RTSS_IO_48		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_CAN5_RX			RTSS CAN 5 receive	
		RTSS_EMAC0_PTP_PPS_O_1_MIRA			RTSS EMAC0 configurable PPS output 1 A	
		RTSS_EMAC0_PTP_AUX_TS_I_0_MIRA			RTSS EMAC0 trigger 0 A for Auxiliary snapshot	
		RTSS_CC_GP4_CLK_MIRB			RTSS Global general-purpose clock 4 B	
AH4	RTSS_IO_49		RTSS_PX_3	PU:nppdkp	RTSS domain configurable I/O	N
		RTSS_CAN6_TX			RTSS CAN 6 transmit	
		RTSS_EMAC0_PTP_PPS_O_0_MIRA			RTSS EMAC0 configurable PPS output 0 A	
AH2	RTSS_IO_50		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_CAN6_RX			RTSS CAN 6 receive	
		RTSS_EMAC0_PTP_PPS_O_0_MIRB			RTSS EMAC0 configurable PPS output 0 B	

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Table 2-4 Pin descriptions – RTSS I/O (cont.)

Pin number	RTSS I/O	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup function
		RTSS_CC_GP5_CLK_MIRA			RTSS Global general-purpose clock 5 A	
AJ5	RTSS_IO_51		RTSS_PX_3	PU:nppdkp	RTSS domain configurable I/O	N
		RTSS_CAN7_TX			RTSS CAN 7 transmit	
		RTSS_EMAC0_PTP_PPS_O_1_MIRB			RTSS EMAC0 configurable PPS output 1 B	
		RTSS_FORCED_USB_BOOT (ES1 only)			Boot strap to enter USB0 emergency download mode for RTSS domain. See *QCS9075 Technical Reference Manual* (80-73418-5) (to be released) for details.	
AJ3	RTSS_IO_52		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_CAN7_RX			RTSS CAN 7 receive	
		RTSS_CC_GP5_CLK_MIRB			RTSS Global general-purpose clock 5 B	
AV4	RTSS_IO_53		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
AJ1	RTSS_IO_54		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
AK4	RTSS_IO_55		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_EMAC0_PTP_PPS_O_2			RTSS EMAC0 configurable PPS output 2	
AK2	RTSS_IO_56		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_EMAC0_PTP_AUX_TS_I_0_MIRB			RTSS EMAC0 trigger 0 B for Auxiliary snapshot	
		RTSS_EMAC0_PTP_PPS_O_3			RTSS EMAC0 configurable PPS output 3	
AT6	RTSS_IO_57		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_EMAC0_MCG_PST_TRIG_LW[0]			RTSS EMAC0 trigger input 0 for Media clock generation	
AT4	RTSS_IO_58		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_EMAC0_MCG_PST_TRIG_LW[1]			RTSS EMAC0 trigger input 1 for Media clock generation	
AU3	RTSS_IO_59		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_EMAC0_MCG_PST_TRIG_LW[2]			RTSS EMAC0 trigger input 2 for Media clock generation	
		RTSS_CC_GP1_CLK_MIRA			RTSS Global general-purpose clock 1 A	

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Table 2-4 Pin descriptions – RTSS I/O (cont.)

Pin number	RTSS I/O	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup function
AV2	RTSS_IO_60		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_EMAC0_MCG_PST_TRIG_LW[3]			RTSS EMAC0 trigger input 3 for Media clock generation	
		RTSS_CC_GP1_CLK_MIRB			RTSS Global general-purpose clock 1 B	
AU1	RTSS_IO_61		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
AY8	RTSS_IO_62		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
AW9	RTSS_IO_63		RTSS_PX_3	PD:nppukp	Configurable I/O	N
		PRTSS_ERR_N			PMIC RTSS domain error signal active low (internally pulled up to 1.8 V). Indicates PMIC error and resulting PMIC shutdown.	
AV10	RTSS_IO_64		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
AW7	RTSS_IO_65		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	Y
		RTSS_PWR_READY			RTSS power ready	
AV8	RTSS_IO_66		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_SLP_EN			RTSS sleep enable	
J7	RTSS_IO_67		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_OSPI0_CS_N_0			RTSS OSPI0 chip select 0	
K6	RTSS_IO_68		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_OSPI0_DQS			RTSS OSPI0 differential data strobe	
K8	RTSS_IO_69		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
K10	RTSS_IO_70		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_OSPI0_CLK			RTSS OSPI0 clock	
L7	RTSS_IO_71		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_OSPI0_DATA[0]			RTSS OSPI0 data 0	
L9	RTSS_IO_72		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_OSPI0_DATA[1]			RTSS OSPI0 data 1	
M6	RTSS_IO_73		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_OSPI0_DATA[2]			RTSS OSPI0 data 2	

Table 2-4 Pin descriptions – RTSS I/O (cont.)

Pin number	RTSS I/O	Alternate functions	Pad voltage	Pad type	Functional description	Wakeup function
M8	RTSS_IO_74		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_OSPI0_DATA[3]			RTSS OSPI0 data 3	
M10	RTSS_IO_75		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_OSPI0_DATA[4]			RTSS OSPI0 data 4	
N7	RTSS_IO_76		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_OSPI0_DATA[5]			RTSS OSPI0 data 5	
N9	RTSS_IO_77		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_OSPI0_DATA[6]			RTSS OSPI0 data 6	
P10	RTSS_IO_78		RTSS_PX_3	PD:nppukp	RTSS domain configurable I/O	N
		RTSS_OSPI0_DATA[7]			RTSS OSPI0 data 7	

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Table 2-5 Pin descriptions – MD_LPASS

LPASS I/O	Alternate function	Functional description
LPASS_0		(GPIO_126)
	LPI_QUA_MI2S_SCK	LPI quad I^2S clock
LPASS_1		(GPIO_127)
	LPI_QUA_MI2S_WS	LPI quad I^2S word select
LPASS_2		(GPIO_128)
	LPI_QUA_MI2S_DATA0	LPI quad I^2S serial channel 0
LPASS_3		(GPIO_129)
	LPI_QUA_MI2S_DATA1	LPI quad I^2S serial channel 1
LPASS_4		(GPIO_130)
	LPI_QUA_MI2S_DATA2	LPI quad I^2S serial channel 2
LPASS_5		(GPIO_131)
	LPI_QUA_MI2S_DATA3	LPI quad I^2S serial channel 3
	EXT_MCLK1_C	MI2S external MCLK1 C
LPASS_6		(GPIO_132)
	LPI_I2S1_CLK	LPI I2S 1 clock
LPASS_7		(GPIO_133)
	LPI_I2S1_WS	LPI I2S 1 word select
LPASS_8		(GPIO_134)
	LPI_I2S1_DATA0	LPI I2S 1 serial channel 0
LPASS_9		(GPIO_135)
	LPI_I2S1_DATA1	LPI I2S 1 serial channel 1
	EXT_MCLK1_B	MI2S external MCLK1 B
LPASS_10		(GPIO_136)
	LPI_I2S2_CLK	LPI I2S 2 clock
LPASS_11		(GPIO_137)
	LPI_I2S2_WS	LPI I2S 2 word select
LPASS_12		(GPIO_141)
	LPI_I2S4_CLK	LPI I2S 4 clock
LPASS_13		(GPIO_142)
	LPI_I2S4_WS	LPI I2S 4 word select
	EXT_MCLK1_A	MI2S external MCLK1 A
LPASS_14		(GPIO_140)
	EXT_MCLK1_D	MI2S external MCLK1 D
LPASS_15		(GPIO_138)
	LPI_I2S2_DATA0	LPI I2S 2 serial channel 0
LPASS_16		(GPIO_139)
	LPI_I2S2_DATA1	LPI I2S 2 serial channel 1
LPASS_17		(GPIO_143)
	LPI_I2S4_DATA0	LPI I2S 4 serial channel 0

Table 2-5 Pin descriptions – MD_LPASS (cont.)

LPASS I/O	Alternate function	Functional description
LPASS_18		(GPIO_144)
	LPI_I2S4_DATA1	LPI I2S 4 serial channel 1
LPASS_19		(GPIO_145)
	LPI_I2S3_CLK	LPI I2S 3 clock
LPASS_20		(GPIO_146)
	LPI_I2S3_WS	LPI I2S 3 word select
LPASS_21		(GPIO_147)
	LPI_I2S3_DATA0	LPI I2S 3 serial channel 0
LPASS_22		(GPIO_148)
	LPI_I2S3_DATA1	LPI I2S 3 serial channel 1
	EXT_MCLK1_E	MI2S external MCLK1 E

Table 2-6 Pin descriptions – power-supply pins

Pin number	Pin name	Functional description
AA53, AA57, N49, N51, N55, N57, P58, R49, R57, R59, T48, U49, U57, U59, V48, W57, W59, Y58	VDD_APC0	Power for the cluster 0 of Kryo Gold Prime processors
AA37, AA41, AA43, M38, M42, M46, N37, N47, P38, P46, R37, R47, T38, V38, V44, W37, W45, Y38	VDD_APC1	Power for the cluster 1 of Kryo Gold Prime processors
U47	VDD_A_APC_CS_1P2	Power for application processor current sensor 1.2 V analog circuits
AV50	VDD_A_CSI_0_1P2	Power for MIPI CSI0 1.2 V analog circuits
AT50	VDD_A_CSI_0_1_0P9	Power for MIPI CSI0/CSI1 0.9 V analog circuits
AV52	VDD_A_CSI_1_1P2	Power for MIPI CSI1 1.2 V analog circuits
AV54	VDD_A_CSI_2_1P2	Power for MIPI CSI2 1.2 V analog circuits
AT54	VDD_A_CSI_2_3_0P9	Power for MIPI CSI2/CSI3 0.9 V analog circuits
AV56	VDD_A_CSI_3_1P2	Power for MIPI CSI3 1.2 V analog circuits
AU45	VDD_A_DSI_0_0P9	Power for MIPI DSI0 0.9 V analog circuits
AV46, AV48	VDD_A_DSI_0_1_1P2	Power for MIPI DSI0/DSI1 1.2 V analog circuits
AT46	VDD_A_DSI_0_PLL_0P9	Power for MIPI DSI0 PLL 0.9 V
AU49	VDD_A_DSI_1_0P9	Power for MIPI DSI1 0.9 V analog circuits
AT48	VDD_A_DSI_1_PLL_0P9	Power for MIPI DSI1 PLL 0.9 V
M26, M28, M32, M34	VDD_A_EBI_01_0P9	Power for EBI0/EBI1 PHY 0.9 V circuits
M52, M54, M58, M60, R63, U63, V60, W63	VDD_A_EBI_23_45_0P9	Power for EBI2/EBI3/EBI4/EBI5 PHY 0.9 V circuits
K24, K34, K50, K58, N65, V66	VDD_A_EBI_PLL	Power for EBI PHY PLL circuits
AJ59	VDD_A_EDP_0_0P9	Power for EDP 0 0.9 V circuits
AH64	VDD_A_EDP_0_1P2	Power for EDP 0 1.2 V circuits
AK60	VDD_A_EDP_1_0P9	Power for EDP 1 0.9 V circuits

Table 2-6 Pin descriptions – power-supply pins (cont.)

Pin number	Pin name	Functional description
AK64	VDD_A_EDP_1_1P2	Power for EDP 1 1.2 V circuits
AK62	VDD_A_EDP_2_0P9	Power for EDP 2 0.9 V circuits
AL63	VDD_A_EDP_2_1P2	Power for EDP 2 1.2 V circuits
AM62	VDD_A_EDP_3_0P9	Power for EDP 3 0.9 V circuits
AL61	VDD_A_EDP_3_1P2	Power for EDP 3 1.2 V circuits
AK58	VDD_A_NSP0_CS_1P2	Power for HTP0 current sensor 1.2 V circuits
V32	VDD_A_NSP1_CS_1P2	Power for HTP1 current sensor 1.2V circuits
T18, T20, U21	VDD_A_PCIE_0_0P9	Power for PCIe 0 0.9 V circuits
V20, V22, W21, W23	VDD_A_PCIE_1_0P9	Power for PCIe 1 0.9V circuits
T16	VDD_A_PCIE_0_PLL_1P2	Power for PCIe 0 PLL 1.2 V circuits
U13	VDD_A_PCIE_1_PLL_1P2	Power for PCIe 1 PLL 1.2 V circuits
AC65	VDD_A_REFGEN_0P875	Power for high-speed interface reference generation circuits – 0.875 V
AD66	VDD_A_REFGEN_1P2	Power for high-speed interface reference generation circuits – 1.2 V
Y22	VDD_A_SGMII_0_0P9	Power for serial gigabit media-independent interface 0 0.9 V
AA19	VDD_A_SGMII_0_1P2	Power for serial gigabit media-independent interface 0 1.2 V
AA21	VDD_A_SGMII_1_0P9	Power for serial gigabit media-independent interface 1 0.9 V
AB20	VDD_A_SGMII_1_1P2	Power for serial gigabit media-independent interface 1 1.2 V
AH60, AF60	VDD_A_UFS_0_0P9	Power for the UFS 0.9 V analog circuits
AG63, AG61	VDD_A_UFS_0_1P2	Power for the UFS 1.2 V analog circuits
K36	VDD_A_USBHS_0_0P9	Power for USB high-speed 0 0.9 V circuits
J37	VDD_A_USBHS_0_1P8	Power for USB high-speed 0 1.8 V circuits
J39	VDD_A_USBHS_0_3P1	Power for USB high-speed 0 3.1 V circuits
K40	VDD_A_USBHS_1_0P9	Power for USB high-speed 1 0.9 V circuits
J41	VDD_A_USBHS_1_1P8	Power for USB high-speed 1 1.8 V circuits
J43	VDD_A_USBHS_1_3P1	Power for USB high-speed 1 3.1 V circuits
L45	VDD_A_USBHS_2_0P9	Power for USB high-speed 2 0.9 V circuits
K46	VDD_A_USBHS_2_1P8	Power for USB high-speed 2 1.8 V circuits
K48	VDD_A_USBHS_2_3P1	Power for USB high-speed 2 3.1 V circuits
L39	VDD_A_USBSS_0_0P9	Power for USB super-speed 0 0.9 V circuits
K38	VDD_A_USBSS_0_1P2	Power for USB super-speed 0 1.2 V circuits
L43	VDD_A_USBSS_1_0P9	Power for USB super-speed 1 0.9 V circuits
K42	VDD_A_USBSS_1_1P2	Power for USB super-speed 1 1.2 V circuits

Table 2-6 Pin descriptions – power-supply pins (cont.)

Pin number	Pin name	Functional description
AA35, AB38, AB40, AB44, AB46, AC35, AD50, AD52, AE49, AG49, AJ49, AK50, T36, U35, V34, W35, Y36, Y46	VDD_CX	Power for digital core circuits
AC55, AC59, AC63, AD54, AD56, AD58, AD60, AD64	VDD_CX_LPI	Power for Low-power island digital core circuits
AA61, L23, L25, L27, L31, L33, L35, L49, L51, L53, L57, L59, L61, N61, P62, T62, V62, Y62	VDD_D_EBI	Power for EBI digital circuits
AH24, AH26, AH30, AJ23, AJ25, AJ33, AK34, AL23, AL25, AM36, AN23, AN25, AN35, AP36, AR23, AR25, AR27, AR29, AR31, AR33, AR35, AT26, AT30, AT34, AU29, AU31, AU35, AV24, AV28, AV34	VDD_GFX	Power for graphics
M22, M24, M30, M36	VDD_IO_EBI_01	Power for EBI0/EBI1 I/O circuits
AA63, M48, M50, M56, N59, R61, U61, W61	VDD_IO_EBI_23_45	Power for EBI2/EBI3/EBI4/EBI5 I/O circuits
AE35, AF36, AG35, AG37, AH34, AH46, AJ41, AJ45, AK40, AK44, AL45, AM38, AN45, AP38, AR39, AR41, AR45, AR47, AT38, AT42, AU39, AU43, AV38, AV42	VDD_MM	Power for multimedia subsystem circuits
AA51, AB48, AB50, AC47, AC51, AD46, AK46, AL47, AM46, W47, Y48	VDD_MX_A	Power for always-ON memory circuits
AA33, AB34, AC33, AD34, AE33, ,AF48, AG47, AH38, AH48, AJ37, AK36, AL37	VDD_MX_C	Power for collapsible memory circuits
AB54, AB56, AB58, AB60, AB64	VDD_MX_LPI	Power for Low-power island memory circuit
AE53, AE55, AE57, AF58, AG57, AJ51, AJ53, AJ57, AK54, AK56, AM48, AM58, AM60, AP48, AP58, AP60, AR49, AR51, AR55, AR57, AR61	VDD_NSP0	Power for Hexagon Tensor Processor 0
AA25, AB24, AC25, AC29, N21, N25, N27, N31, N33, P22, P24, P34, T22, T24, T34, V24, V28, V30, W25, W29, W31	VDD_NSP1	Power for Hexagon Tensor Processor 1
AB68	VDD_PX0	Power for pad group 0
K30, K54, T66, Y66	VDD_PX1	Power for pad group 1
AG67	VDD_PX10	Power for pad group 10
AE63, J35	VDD_PX11	Power for pad group 11
AB66, AU21, AV32, AV58, AW45, J33	VDD_PX3	Power for pad group 3
AB16	VDD_PX7	Power for pad group 7
AF66	VDD_PX9	Power for pad group 9
AV60, AA67	VDD_QFPROM	Power for programming the QFPROM
AC21	VDD_QFPROM_RTSS	Power for programming the QFPROM RTSS

Table 2-6 Pin descriptions – power-supply pins (cont.)

Pin number	Pin name	Functional description
AE31, AF24, AF28, AF32, AG23, AG27, AG31, AH32	VDD_RTSS_CX	Power for RTSS digital core circuits
AD26, AD30, AE23, AE27, AE29	VDD_RTSS_MX	Power for RTSS On-chip memory circuits
AT20	VDD_RTSS_PX0	Power for RTSS pad group 0
AR19	VDD_RTSS_PX11	Power for RTSS pad group 11
AF18, AK20, AP20	VDD_RTSS_PX3	Power for RTSS pad group 3
AH20	VDD_RTSS_PX8	Power for RTSS pad group 8
AD20	VBIAS_RTSS_RGMII	Power for RTSS_RGMII reference circuits; 0.85 V

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Pin descriptions – ground pins

Table 2-7 Pin descriptions – ground pins

Pin number	Pin name	Functional description
A9, A29, A47, A67, A75, A77, AA13, AA15,AA17, AA23, AA39, AA45, AA47, AA49, AA55, AA59, AA65, AA75, AA79, AB8, AB12, AB14, AB18, AB22, AB36, AB42, AB52, AB62, AB70, AB72, AB76, AB78, AC1, AC5, AC11, AC13, AC15, AC17, AC19, AC23, AC27, AC31, AC49, AC53, AC57, AC61, AC67, AC69, AC71, AC75, AC79, AD8, AD12, AD14, AD16, AD18, AD22, AD24, AD28, AD32, AD36, AD48, AD62, AD68, AD70, AD74, AD78, AE11, AE13, AE15, AE17, AE19, AE25, AE47, AE51, AE59, AE61, AE65, AE67, AE69, AE71, AE75, AE79, AF8, AF10, AF12, AF14, AF16, AF22, AF26, AF30, AF34, AF46, AF62, AF64, AF68, AF72, AF76, AF78, AG1, AG7, AG11, AG13, AG15, AG17, AG19, AG25, AG29, AG33, AG59, AG65, AG69, AG73, AG79, AH6, AH12, AH14, AH16, AH18, AH28, AH36, AJ55, AH58, AH62, AH66, AH68, AH70, AH76, AJ11, AJ13, AJ15, AJ17, AJ19, AJ21, AJ35, AJ39, AJ43, AJ47, AJ61, AJ63, AJ65, AJ67, AJ69, AJ75, AJ79, AK8, AK12, AK14, AK16, AK18, AK22, AK24, AK38, AK42, AK48, AK52, AK66, AK68, AK70, AK74, AL1, AL5, AL11, AL13, AL15, AL17, AL19, AL21, AL35, AL39, AL59, AL65, AL67, AL69, AL79, AM12, AM14, AM16, AM18, AM20, AM22, AM24, AM64, AM66, AM68, AM74, AN1, AN5, AN11, AN13, AN15, AN17, AN19, AN21, AN37, AN39, AN47, AN59, AN61, AN63, AN65, AN67, AN69, AN79, AP4, AP6, AP12, AP14, AP16, AP18, AP22, AP24, AP46, AP62, AP64, AP66, AP68, AP74, AR5, AR11, AR13, AR15, AR17, AR37, AR43, AR53, AR59, AR65, AR67, AR69, AR79, AT10, AT12, AT14, AT16, AT18, AT24, AT28, AT32, AT36, AT40, AT44, AT52, AT56, AT58, AT60, AT64, AT66, AT68, AT74, AU7, AU9, AU11, AU13, AU17, AU19, AU27, AU33, AU37, AU41, AU47, AU51, AU53, AU55, AU57, AU59, AU61, AU63, AU65, AU67, AU69, AV14, AV16, AV18, AV20, AV22, AV26, AV30, AV36, AV40, AV44, AV62, AV64, AV66, AV68, AV74, AV78, AW13, AW15, AW17, AW19, AW21, AW23, AW25, AW27, AW29, AW31, AW33, AW35, AW37, AW39, AW41, AW43, AW47, AW49, AW51, AW53, AW55, AW57, AW59, AW61, AW63, AW65, AW67, AW69, AY6, AY42, AY44, AY46, AY48, AY50, AY52, AY54, AY56, AY58, AY60, AY66, AY68, AY70, AY72, AY76, AY78, B6, B12, B14, B18, B22, B24, B26, B32, B34, B36, B38, B40, B42, B44, B50, B52, B54, B58, B62, B64, B70, B72, B76, BA1, BA41, BA43, BA49, BA51, BA53, BA55, BA65, BA67, BA69, BA71, BA77, BB24, BB50, BB52, BB66, BB68, BC31, BC35, BC45, BC59, BC61, BC63, BC77, BD6, BD14, BD22, BD28, BD42, BD44, BD46, BD48, BD54, BD60, BD62, BD64, BE39, BE45, BE47, BE49, BE55, BE57, BE59, BE65, BE67, BE69, BF36, BF46, BF56, BF74, BG5, BG11, BG17, BG23, BG31, BG41, BG51, BG61, BG75, C3, C9, C17, C27, C29, C47, C49, C67, C75, C79, D6, D8, D12, D22, D24, D32, D34, D36, D38, D40, D42, D44, D52, D54, D62, D64, D68, D70, D72, D76, D78, E3, E11, E17, E27, E29, E47, E49, E59, E65, E75, E79, F4, F6, F8, F14, F22, F26, F32, F34, F36, F38, F40, F42, F44, F50, F54, F62, F68, F70, F74, F78, G3, G11, G17, G23, G29, G35, G47, G53, G59, G65, G71, G75, G79, H2, H4, H6, H8, H10, H14, H16, H18, H20, H22, H24, H26, H30, H32, H38, H40, H42, H44, H46, H50, H54, H56, H58, H60, H62, H66, H68, H70, H74, H76, J9, J11, J13, J15, J17, J19, J21, J23, J25, J27, J29, J31, J47, J55, J57, J59, J61, J63, J65, J67, J69, J73, J79, K12, K16, K18, K20, K22, K26, K28, K32, K52, K56, K60, K62, K64, K68, K70, K76, L11, L13, L15, L17, L19, L21, L29, L37, L41, L47, L55, L63, L65, L67, L73, L79, L81, M12, M14, M16, M18, M20, M40, M44, M62, M64, M66, M68, M70, M74, M76, N11, N13, N15, N17, N23, N29, N35, N53, N63, N67, N69, N73, N79, P6, P12, P14, P16, P20, P36, P48, P60, P64, P66, P68, P70, P76, P78, R1, R11, R13, R15, R17, R19, R21, R23, R35, R65, R67, R69, R73, R75, R79, T12, T14, T46, T58, T60, T64, T68, T72, T76, U7, U11, U23, U37, U65, U67, U69, U75, U79, V6, V10, V12, V14, V26, V36, V46, V58, V64, V68, V70, V72, V78, W1, W11, W13, W27, W33, W49, W65, W67, W69, W75, W81, Y6, Y8, Y12, Y14, Y20, Y24, Y34, Y44, Y60, Y64, Y68, Y70, Y72, Y78,	GND	Ground

Pin descriptions – DNC pins

Table 2-8 Pin descriptions – DNC pins

Pin number	Pin name	Functional description
AR21, BB40, BA39, B78, C77, J53, J45, AE21, AG21, AH22, AU23, AT62, P18, H28, H64, AA69, BA29, AA9, H34, H52, J49, AJ81, BB28, AY10, J51, K44, AU25, AR63, N19, AF20, AT22, A1, A3, A79, A81, B2, B80, BE1, BE81, BF2, BF80, BG1, BG3, BG79, BG81, C1, C81	DNC	Do not connect; do not connect externally.

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings shown in the following table reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Operating conditions.

Table 3-1 Absolute maximum ratings

Power supply	Description	Min	Max	Unit
VDD_APC0	Power for the cluster 0 of Kryo Gold Prime processors	-0.3	1.133	V
VDD_APC1	Power for the cluster 1 of Kryo Gold Prime processors	-0.3	1.133	V
VDD_A_APC_CS_1P2	Power for application processor current sensor 1.2 V analog circuits	-0.3	1.430	V
VDD_A_NSP0_CS_1P2	Power for HTP0 current sensor 1.2 V circuits			
VDD_A_NSP1_CS_1P2	Power for HTP1 current sensor 1.2 V circuits			
VDD_PX11	Power for pad group 11			
VDD_RTSS_PX11	Power for RTSS pad group 11			
VDD_CX	Power for digital core circuits	-0.3	1.133	V
VDD_D_EBI	Power for EBI digital circuits			
VDD_RTSS_CX	Power for RTSS digital core circuits			
VDD_CX_LPI	Power for Low-power island digital core circuits	-0.3	1.133	V
VDD_GFX	Power for graphics	-0.3	1.133	V
VDD_MM	Power for multimedia subsystem circuits	-0.3	1.133	V
VDD_MX_A	Power for always-ON memory circuits	-0.3	1.133	V
VDD_RTSS_MX	Power for RTSS On-chip memory circuits			
VDD_MX_C	Power for collapsible memory circuits	-0.3	1.133	V
VDD_MX_LPI	Power for Low-power island memory circuit	-0.3	1.133	V
VDD_NSP0	Power for Hexagon Tensor Processor 0	-0.3	1.300	V
VDD_NSP1	Power for Hexagon Tensor Processor 1	-0.3	1.300	V
VDD_PX0	Power for pad group 0	-0.3	2.090	V
VDD_RTSS_PX0	Power for RTSS pad group 0			
VDD_PX1	Power for pad group 1	-0.3	1.232	V
VDD_PX10	Power for pad group 10	-0.3	1.375	V
VDD_PX3	Power for pad group 3	-0.3	2.090	V
VDD_PX7	Power for pad group 7			
VDD_QFPROM	Power for programming the QFPROM			
VDD_RTSS_PX3	Power for RTSS pad group 3			
VDD_QFPROM_RTSS	Power for programming the QFPROM RTSS			
VDD_PX9	Power for pad group 9	-0.3	1.375	V
VDD_RTSS_PX8	Power for RTSS pad group 8	-0.3	2.915	V

Table 3-1 Absolute maximum ratings (cont.)

Power supply	Description	Min	Max	Unit
VBIAS_RTSS_RGMII	Power for RTSS_RGMII reference circuits; 0.85 V	-0.3	0.990	V
VDD_A_CSI_0_1_0P9	Power for MIPI CSI0/CSI1 0.9 V analog circuits	-0.3	1.012	V
VDD_A_CSI_2_3_0P9	Power for MIPI CSI2/CSI3 0.9 V analog circuits			
VDD_A_DSI_0_0P9	Power for MIPI DSI0 0.9 V analog circuits			
VDD_A_DSI_0_PLL_0P9	Power for MIPI DSI0 PLL 0.9 V			
VDD_A_DSI_1_0P9	Power for MIPI DSI1 0.9 V analog circuits			
VDD_A_DSI_1_PLL_0P9	Power for MIPI DSI1 PLL 0.9 V			
VDD_A_EDP_0_0P9	Power for EDP 0 0.9 V circuits			
VDD_A_EDP_1_0P9	Power for EDP 1 0.9 V circuits			
VDD_A_EDP_2_0P9	Power for EDP 2 0.9 V circuits			
VDD_A_EDP_3_0P9	Power for EDP 3 0.9 V circuits			
VDD_A_REFGEN_0P875	Power for high-speed interface reference generation circuits – 0.875 V			
VDD_A_SGMII_0_0P9	Power for serial gigabit media-independent interface 0 - 0.9 V			
VDD_A_SGMII_1_0P9	Power for serial gigabit media-independent interface 1 - 0.9 V			
VDD_A_UFS_0_0P9	Power for the UFS0 0.9 V analog circuits			
VDD_A_UFS_1_0P9	Power for the UFS1 0.9 V analog circuits			
VDD_A_CSI_0_1P2	Power for MIPI CSI0 1.2 V analog circuits	-0.3	1.375	V
VDD_A_CSI_1_1P2	Power for MIPI CSI1 1.2 V analog circuits			
VDD_A_CSI_2_1P2	Power for MIPI CSI2 1.2 V analog circuits			
VDD_A_CSI_3_1P2	Power for MIPI CSI3 1.2 V analog circuits			
VDD_A_DSI_0_1_1P2	Power for MIPI DSI0/DSI1 1.2 V analog circuits			
VDD_A_EDP_0_1P2	Power for EDP 0 1.2 V circuits			
VDD_A_EDP_1_1P2	Power for EDP 1 1.2 V circuits			
VDD_A_EDP_2_1P2	Power for EDP 2 1.2 V circuits			
VDD_A_EDP_3_1P2	Power for EDP 3 1.2 V circuits			
VDD_A_PCIE_0_PLL_1P2	Power for PCIe 0 PLL 1.2 V circuits			
VDD_A_PCIE_1_PLL_1P2	Power for PCIe 1 PLL 1.2 V circuits			
VDD_A_REFGEN_1P2	Power for high-speed interface reference generation circuits – 1.2 V			
VDD_A_SGMII_0_1P2	Power for serial gigabit media-independent interface 0 - 1.2 V			
VDD_A_SGMII_1_1P2	Power for serial gigabit media-independent interface 1 - 1.2 V			
VDD_A_UFS_0_1P2	Power for the UFS0 1.2 V analog circuits			
VDD_A_UFS_1_1P2	Power for the UFS1 1.2 V analog circuits			
VDD_A_USBSS_0_1P2	Power for USB super-speed 0 1.2 V circuits			
VDD_A_USBSS_1_1P2	Power for USB super-speed 1 1.2 V circuits			
VDD_A_USBHS_0_0P9	Power for USB high-speed 0 0.9 V circuits	-0.3	1.012	V
VDD_A_USBHS_1_0P9	Power for USB high-speed 1 0.9 V circuits			
VDD_A_USBHS_2_0P9	Power for USB high-speed 2 0.9 V circuits			
VDD_A_USBSS_0_0P9	Power for USB super-speed 0 0.9 V circuits			
VDD_A_USBSS_1_0P9	Power for USB super-speed 1 0.9 V circuits			
VDD_A_USBHS_0_3P1	Power for USB high-speed 0 3.1 V circuits	-0.3	3.520	V

Table 3-1 Absolute maximum ratings (cont.)

Power supply	Description	Min	Max	Unit
VDD_A_USBHS_1_3P1	Power for USB high-speed 1 3.1 V circuits			
VDD_A_USBHS_2_3P1	Power for USB high-speed 2 3.1 V circuits			
VDD_A_USBHS_0_1P8	Power for USB high-speed 0 1.8 V circuits	-0.3	2.145	V
VDD_A_USBHS_1_1P8	Power for USB high-speed 1 1.8 V circuits			
VDD_A_USBHS_2_1P8	Power for USB high-speed 2 1.8 V circuits			
VDD_A_PCIE_0_0P9	Power for PCIe 0.9 V circuits	-0.3	1.012	V
VDD_A_PCIE_1_0P9				
VDD_A_EBI_01_0P9	Power for EBI0/EBI1 circuits	-0.3	1.133	V
VDD_A_EBI_PLL	Power for EBI PHY PLL circuits			
VDD_A_EBI_23_45_0P9	Power for EBI2/EBI3/EBI4/EBI5 PHY 0.9 V circuits			
VDD_IO_EBI_01	Power for EBI0/EBI1 I/O circuits	-0.3	0.627	V
VDD_IO_EBI_23_45	Power for EBI2/EBI3/EBI4/EBI5 I/O circuits			
T_s	Storage temperature [a, b]	-55	150	°C

[a] The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.

[b] For devices shipped in tape and reel, the storage temperature range is [+15°C~35°C] and <-90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

The QCS9075 meets all performance specifications, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions for voltage rails with AVS Type - 1

Parameter		Min	Max	Unit
Power supply voltages				
VDD_APC0	Power for the cluster 0 of Kryo Gold Prime processors			
	Active	0.576	1.030	V
VDD_APC1	Power for the cluster 1 of Kryo Gold Prime processors			
	Active	0.576	1.030	V
VDD_CX	Power for digital core circuits			
VDD_D_EBI	Power for EBI digital circuits			
VDD_RTSS_CX	Power for RTSS digital core circuits			
	Active	0.560	1.030	V
	Retention [a]	0.352	0.480	V
VDD_CX_LPI	Power for Low-power island digital core circuits			
	Active	0.560	1.030	V
	Retention [a]	0.352	0.480	V
VDD_GFX	Power for graphics			
	Active	0.560	1.030	V
VDD_MM	Power for multimedia subsystem circuits			

Table 3-2 Operating conditions for voltage rails with AVS Type - 1 (cont.)

Parameter		Min	Max	Unit
	Active	0.560	1.030	V
VDD_MX_A	Power for always-ON memory circuits			
VDD_RTSS_MX	Power for RTSS On-chip memory circuits			
	Active	0.716	1.030	V
	Retention [a]	0.504	0.680	V
VDD_MX_C	Power for collapsible memory circuits			
	Active	0.716	1.030	V
VDD_MX_LPI	Power for Low-power island memory circuit			
	Active	0.695	1.030	V
	Retention [a]	0.504	0.680	V
VDD_NSP0	Power for Hexagon Tensor Processor 0			
	Active	0.560	1.030	V
VDD_NSP1	Power for Hexagon Tensor Processor 1			
	Active	0.560	1.030	V
VDD_A_EBI_0P9	Power for EBI PHY 0.9 V circuits			
VDD_A_EBI_PLL	Power for EBI PHY PLL circuits			
VDD_A_EBI_23_45_0P9	Power for EBI2/EBI3/EBI4/EBI5 I/O circuits			
	Active	0.835	1.030	V
	Retention [a]	0.352	0.480	V

[a] The retention voltage is the PMIC output setting and it is static. There is no scaling.

Table 3-3 Operating conditions for non AVS voltage rails

Parameter [a]		Min	Typ [b]	Max	Unit
Power supply voltages					
VDD_A_APC_CS_1P2	Power for application processor current sensor 1.2 V analog circuits	1.100	1.200	1.300	V
VDD_A_NSP0_CS_1P2	Power for HTP0 current sensor 1.2 V circuits				
VDD_A_NSP1_CS_1P2	Power for HTP1 current sensor 1.2 V circuits				
VDD_PX11	Power for pad group 11				
VDD_RTSS_PX11	Power for RTSS pad group 11				
VDD_PX0	Power for pad group 0	1.700	1.800	1.900	V
VDD_RTSS_PX0	Power for RTSS pad group 0				
VDD_PX1	Power for pad group 1	1.010	1.100	1.120	V
VDD_PX10	Power for pad group 10	1.100	1.200	1.250	V
VDD_PX3	Power for pad group 3	1.700	1.800	1.900	V
VDD_PX7	Power for pad group 7				
VDD_QFPROM	Power for programming the QFPROM				
VDD_RTSS_PX3	Power for RTSS pad group 3				
VDD_QFPROM_RTSS	Power for programming the QFPROM RTSS				

Table 3-3 Operating conditions for non AVS voltage rails (cont.)

Parameter [a]		Min	Typ [b]	Max	Unit
Power supply voltages					
VDD_PX9	Power for pad group 9	1.100	1.200	1.250	V
VDD_RTSS_PX8	Power for RTSS pad group 8	1.700	1.800	1.900	V
		2.350	2.500	2.650	V
VBIAS_RTSS_RGMII	Power for RTSS_RGMII reference circuits; 0.85 V	0.800	0.850	0.900	V
VDD_A_CSI_0_1_0P9	Power for MIPI CSI0/CSI1 0.9 V analog circuits	0.830	0.880	0.920	V
VDD_A_CSI_2_3_0P9	Power for MIPI CSI2/CSI3 0.9 V analog circuits				
VDD_A_DSI_0_0P9	Power for MIPI DSI0 0.9 V analog circuits				
VDD_A_DSI_0_PLL_0P9	Power for MIPI DSI0 PLL 0.9 V				
VDD_A_DSI_1_0P9	Power for MIPI DSI1 0.9 V analog circuits				
VDD_A_DSI_1_PLL_0P9	Power for MIPI DSI1 PLL 0.9 V				
VDD_A_EDP_0_0P9	Power for EDP 0 0.9 V circuits				
VDD_A_EDP_1_0P9	Power for EDP 1 0.9 V circuits				
VDD_A_EDP_2_0P9	Power for EDP 2 0.9 V circuits				
VDD_A_EDP_3_0P9	Power for EDP 3 0.9 V circuits				
VDD_A_REFGEN_0P875	Power for high-speed interface reference generation circuits – 0.875 V				
VDD_A_SGMII_0_0P9	Power for serial giga bit media-independent interface 0 - 0.9 V				
VDD_A_SGMII_1_0P9	Power for serial giga bit media-independent interface 1 - 0.9 V				
VDD_A_UFS_0_0P9	Power for the UFS0 0.9 V analog circuits				
VDD_A_UFS_1_0P9	Power for the UFS1 0.9 V analog circuits				
VDD_A_CSI_0_1P2	Power for MIPI CSI0 1.2 V analog circuits	1.150	1.200	1.250	V
VDD_A_CSI_1_1P2	Power for MIPI CSI1 1.2 V analog circuits				
VDD_A_CSI_2_1P2	Power for MIPI CSI2 1.2 V analog circuits				
VDD_A_CSI_3_1P2	Power for MIPI CSI3 1.2 V analog circuits				
VDD_A_DSI_0_1_1P2	Power for MIPI DSI0/DSI1 1.2 V analog circuits				
VDD_A_EDP_0_1P2	Power for EDP 0 1.2 V circuits				
VDD_A_EDP_1_1P2	Power for EDP 1 1.2 V circuits				
VDD_A_EDP_2_1P2	Power for EDP 2 1.2 V circuits				
VDD_A_EDP_3_1P2	Power for EDP 3 1.2 V circuits				
VDD_A_PCIE_0_PLL_1P2	Power for PCIe 0 PLL 1.2 V circuits				
VDD_A_PCIE_1_PLL_1P2	Power for PCIe 1 PLL 1.2 V circuits				
VDD_A_REFGEN_1P2	Power for high-speed interface reference generation circuits – 1.2 V				
VDD_A_SGMII_0_1P2	Power for serial giga bit media-independent interface 0 - 1.2 V				
VDD_A_SGMII_1_1P2	Power for serial giga bit media-independent interface 1 - 1.2 V				
VDD_A_UFS_0_1P2	Power for the UFS0 1.2 V analog circuits				
VDD_A_UFS_1_1P2	Power for the UFS1 1.2 V analog circuits				
VDD_A_USBSS_0_1P2	Power for USB super-speed 0 1.2 V circuits				
VDD_A_USBSS_1_1P2	Power for USB super-speed 1 1.2 V circuits				

Table 3-3 Operating conditions for non AVS voltage rails (cont.)

Parameter [a]		Min	Typ [b]	Max	Unit
Power supply voltages					
VDD_A_USBHS_0_0P9	Power for USB high-speed 0 0.9 V circuits	0.830	0.880	0.920	V
VDD_A_USBHS_1_0P9	Power for USB high-speed 1 0.9 V circuits				
VDD_A_USBHS_2_0P9	Power for USB high-speed 2 0.9 V circuits				
VDD_A_USBSS_0_0P9	Power for USB super-speed 0 0.9 V circuits				
VDD_A_USBSS_1_0P9	Power for USB super-speed 1 0.9 V circuits				
VDD_A_USBHS_0_3P1	Power for USB high-speed 0 3.1 V circuits	2.970	3.072	3.200	V
VDD_A_USBHS_1_3P1	Power for USB high-speed 1 3.1 V circuits				
VDD_A_USBHS_2_3P1	Power for USB high-speed 2 3.1 V circuits				
VDD_A_USBHS_0_1P8	Power for USB high-speed 0 1.8 V circuits	1.650	1.800	1.950	V
VDD_A_USBHS_1_1P8	Power for USB high-speed 1 1.8 V circuits				
VDD_A_USBHS_2_1P8	Power for USB high-speed 2 1.8 V circuits				
VDD_A_PCIE_0_0P9	Power for PCIe 0.9 V circuits	0.830	0.912	0.920	V
VDD_A_PCIE_1_0P9					
VDD_IO_EBI	Power for EBI I/O circuits	0.470	0.500	0.570	V
VDD_IO_EBI_23_45	Power for EBI2/EBI3/EBI4/EBI5 I/O circuits				
Thermal Conditions					
T_A	Ambient operating temperature	-40	–	85 [c]	°C
T_J	Junction operating temperature	–	–	115	°C

[a] Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
[b] Typical voltages represent the recommended output settings of the companion PMIC device.
[c] The T_J max specification must be met.

3.3 Average operating current

This information will be included in future version of this document.

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3.4 Power-on circuits and power sequence

Dedicated circuits continuously monitor several events that might trigger a power-on sequence. If any of these events occur, the PMIC circuits are powered on, the system's available power sources are determined, the correct source is enabled, and the SoC is taken out of reset.

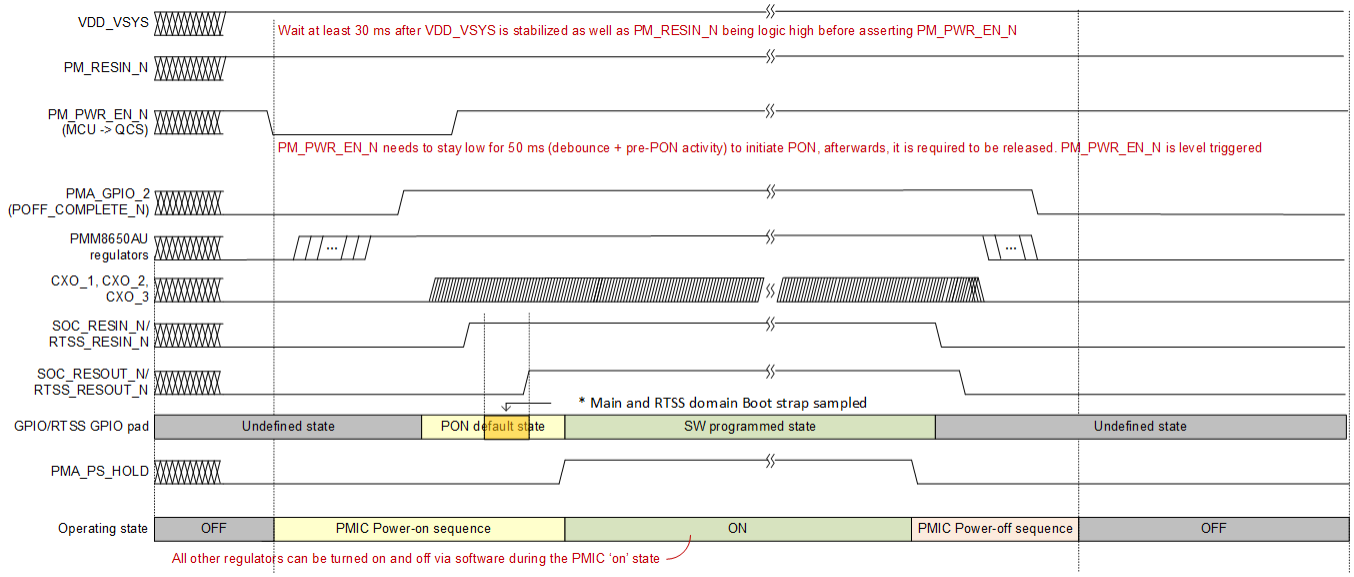


Figure 3-1 QCS9075 and PMIC power-on sequence

3.5 Digital logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage.

- Some are dedicated for interconnections between the QCS9075 device and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I²C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.
- Back powering protection is not supported in digital pads unless otherwise specified in the following table. All non-bpp digital pads must be kept at less than 50 mV and with a maximum of 1 µA current being injected into the pad to avoid potential back-power scenarios.

Table 3-4 Digital I/Os specified in this section

Pad voltage	Usage	Table
1.8 V	VDD_PX0, VDD_RTSS_PX0, VDD_PX3, VDD_RTSS_PX3	Table 3-5
1.8 V	VDD_RTSS_PX8	Table 3-6 and Table 3-7
2.5 V		
1.2 V	VDD_PX9/VDD_PX10	Table 3-8

Table 3-5 DC specification of 1.8 V I/Os

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDD_PXx	VDD_PXx [a] + 0.3	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3	0.35 × VDD_PXx [a]	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDD_PXx	VDD_PXx [a] +0.3	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3	0.3 × VDD_PXx [a]	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN= low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I_{IH}	Input high leakage current	–	3	µA
I_{IL}	Input low leakage current	-1	–	µA
I_{OZH}	High-level, tri-state leakage current	–	3	µA
I_{OZL}	Low-level, tri-state leakage current	-1	–	µA
R_{PD}	Pull-down resistance	20k	60k	Ω
R_{PU}	Pull-up resistance	20k	60k	Ω
R_{KP}	Bus keeper resistor	20k	60k	Ω
V_{OH}	High-level output voltage, CMOS	VDD_PXx [a] -0.45	VDD_PXx [a]	V
V_{OL}	Low-level output voltage, CMOS	0.0	0.45	V

[a] VDD_PXx can be VDD_PX0, VDD_RTSS_PX0, VDD_PX3, VDD_RTSS_PX3 depending on the pad group.

Table 3-6 DC specifications for RGMII 2.5 V mode (VDD_RTSS_PX8)

Parameter	Description	Min	Max	Unit
V_{OL}	Low-level output voltage	-0.3	0.4	V
V_{OH}	High-level output voltage	2	VDD_PXx + 0.3	V
V_{IL}	Low-level input voltage	–	0.7	V
V_{IH}	High-level input voltage	1.7	–	V
V_{HYS}	Input Hysteresis	100	-	mV
$R_{PULL-UP}$	Pull-up resistance	20	50	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	20	50	kΩ
$R_{KEEPERUP}$	Keeper-up resistance	20	50	kΩ
$R_{KEEPERDOWN}$	Keeper-down resistance	20	50	kΩ
I_{IL}	Input low leakage current	–	5	µA
I_{IH}	Input high leakage current	-5	–	µA

Table 3-7 DC specifications for RGMII 1.8 V mode (VDD_RTSS_PX8)

Parameter	Description	Min	Max	Unit
V_{OL}	Low-level output voltage	–	0.45	V
V_{OH}	High-level output voltage	VDD_PXx - 0.45	–	V
V_{IL}	Low-level input voltage	-0.3	0.35× VDD_PXx	V
V_{IH}	High-level input voltage	0.65× VDD_PXx	VDD_PXx+ 0.3	V
V_{HYS}	Input Hysteresis	100	–	mV

Table 3-7 DC specifications for RGMII 1.8 V mode (VDD_RTSS_PX8) (cont.)

Parameter	Description	Min	Max	Unit
$R_{PULL-UP}$	Pull-up resistance	20	50	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	20	50	kΩ
$R_{KEEPERUP}$	Keeper-up resistance	20	50	kΩ
$R_{KEEPERDOWN}$	Keeper-down resistance	20	50	kΩ
I_{IL}	Input low leakage current	–	5	µA
I_{IH}	Input high leakage current	-5	–	µA

NOTE There is no industry-standard specification for a 1.8 V RGMII interface. Thus, the above specifications are taken from *JESD8-7A, "1.8 V ± 0.15 V (Normal range) and 1.2 V – 1.95 V (Wide range) Power Supply Voltage and Interface Standard for Non terminated Digital Integrated Circuits"*.

Table 3-8 Digital I/O characteristics for UFS_RESET and UFS_REF_CLK (VDD_PX9/VDD_PX10)

Parameter	Description	Min	Max	Unit
V_{OL}	Low-level output voltage	0	0.25 × VDD_PXx	V
V_{OH}	High-level output voltage	VDD_PXx × 0.75	VDD_PXx	V
$R_{PULL-UP}$	Pull-up resistance	20	60	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	20	60	kΩ
I_{LEAK}	Standby leakage	-10	10	µA

NOTE VDD_PXx can be either VDD_PX9 or VDD_PX10.

Table 3-9 DC specifications for SPMI (VDD_PX0)

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage	0.65 × VDD_PXx	VDD_PXx + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.35 × VDD_PXx	V
V_{SHYS}	Schmitt hysteresis voltage	100	–	mV
I_{IH}	Input high leakage current	–	30	µA
I_{IL}	Input low leakage current	-10	–	µA
I_{OZH}	High-level, tri-state leakage current	–	30	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	µA
R_{pullup}	Pull-up resistance	7.5 K	20 K	Ω
$R_{pulldown}$	Pull-down resistance	10 K	50 K	Ω
$R_{keeperup}$	Keeper-up resistance	7.5 K	20 K	Ω
$R_{keeperdown}$	Keeper-down resistance	10 K	50 K	Ω
V_{OH}	High-level output voltage, CMOS	VDD_PXx - 0.45	VDD_PXx	V
V_{OL}	Low-level output voltage, CMOS	0	0.45	V

Table 3-10 DC specifications for PS_HOLD and MD_PS_HOLD (VDD_PX3)

Parameter	Description	Min	Max	Unit
V_{IH}	High-level input voltage, (hihys_en = LOW)	0.65 × VDD_PXx	VDD_PXx + 0.3 V	V
V_{IL}	Low-level input voltage, (hihys_en = LOW)	-0.3	0.35 × VDD_PXx	V
V_{IH}	High-level input voltage, (hihys_en = HIGH)	0.7 × VDD_PXx	VDD_PXx + 0.3 V	V
V_{IL}	Low-level input voltage, (hihys_en = HIGH)	-0.3	0.3 × VDD_PXx	V
V_{SHYS}	Schmitt hysteresis, (hihys_en = LOW)	100	–	mV
V_{SHYS}	Schmitt hysteresis, (hihys_en = HIGH)	300	–	mV
IIH	Input high leakage current	–	20	µA
IL	Input low leakage current	-1	–	µA
IOZH	High-level, tri-state leakage current	–	20	µA
OZL	Low-level, tri-state leakage current	-1	–	µA
RPD	Pull-down resistance	10 K	50 K	Ω
R PU	Pull-up resistance	3 K	20 K	Ω
RKP	Bus keeper resistor	3 K	50 K	Ω
VOH	High-level output voltage	VDD_PXx - 0.45	VDD_PXx	V
VOL	Low-level output voltage	0	0.45	V

3.6 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pin design methodologies are included here.

NOTE All QCS9075 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. For more details, see Section 3.6.2.

3.6.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in the following figure.

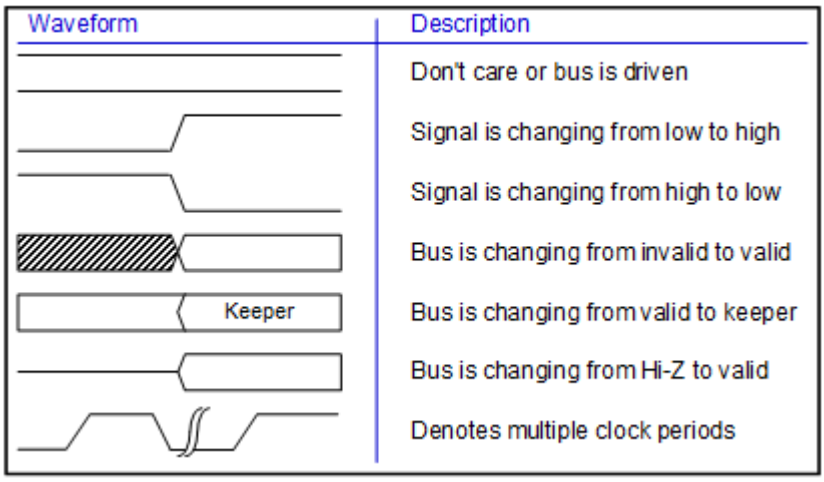


Figure 3-2 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don't care.

3.6.2 Rise and fall time specifications

The testers that characterize QCS9075 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in the following diagram.

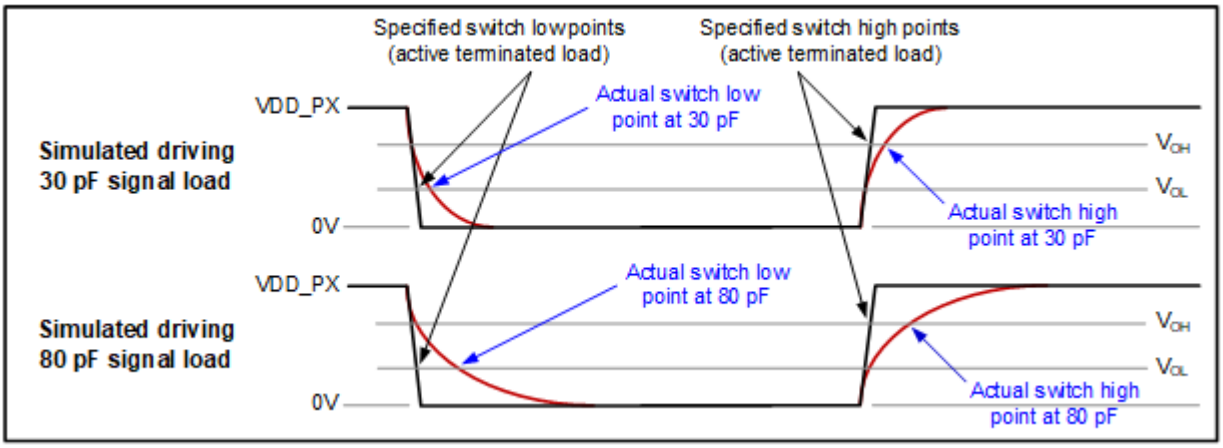


Figure 3-3 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to the parameters that start timing at the QCS9075 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7 Memory support

QCS9075 supports six channel up to 36 GB LPDDR5 memory (JESD209-5C) with maximum speed at 3200 MHz.

3.8 Multimedia

Multimedia parameters requiring performance specifications are addressed in this section.

3.8.1 Camera interfaces

The QCS9075 device supports up to four D-PHY or C-PHY camera interfaces.

Table 3-11 Supported MIPI-CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v3.0	RAW7 is not supported; DPCM predictor 2 is not supported.
MIPI Alliance Specification for D-PHY v1.2	Efficient Packet Delimiter (EPD) for D-PHY is not supported.
MIPI Alliance Specification for C-PHY v1.2	None

3.8.2 Audio support

The audio-related interfaces supported with QCS9075 include:

- I^2S interfaces
- PCM/TDM interfaces

3.8.3 Display support

The QCS9075 device supports one D-PHY or C-PHY display.

Table 3-12 Supported MIPI-DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface 2, v2.1	None
MIPI Alliance Specification for D-PHY v1.2	None
MIPI Alliance Specification for C-PHY v1.1	None

3.8.4 DisplayPort

Table 3-13 Supported DisplayPort standards and exceptions

Applicable standard	Feature exceptions
VESA DisplayPort v1.4	None

3.9 Connectivity

The connectivity functions supported by the QCS9075 that require electrical specifications include:

- USB host/slave support with built-in physical layer (PHY)
- Peripheral component interconnect express (PCIe) interfaces
- Universal flash storage (UFS)
- NOR flash storages (OSPI/QSPI)
- Reduced gigabit media independent interface (RGMII)
- High-speed serial gigabit media-independent interface (HSGMII)
- Inter-IC sound (I^2S) interfaces

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- Pulse-coded modulation (PCM) interfaces
- Time-division multiplexing (TDM) interfaces
- Through proper configuration of 21 main domain (MD) GPIO-based QUP SEs and 5 RTSS domain RTSS_IO-based QUP SEs:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports
- Dedicated I^2C interfaces for camera (CCI I^2C)

Pertinent specifications for these functions are detailed in the following subsections.

NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.9.1 USB interfaces

Table 3-14 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August11, 2014 or later)	None
UTMI specification version 1.05, released on 3/29/2001	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	Attach detection protocol (ADP), role swap protocol (RSP), session request protocol (SRP), and host negotiation protocol (HNP)
USB Serial Bus Specification, Revision 2.0 (April 27, 2000 or later)	None

3.9.2 PCIe interface

Table 3-15 Supported PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI Express Base Specification Revision 4.0	Link configure capability
	Lane margining at receiver
	L0s link state

3.9.3 UFS interface

Table 3-16 Supported UFS standards and exceptions

Applicable standard	Feature exceptions
Universal Flash Storage (UFS), Version 3.1	

3.9.4 HSGMII interface

Table 3-17 Supported HSGMII standards and exceptions

Applicable standard	Feature exceptions
IEEE 802.3 section 47	None

3.9.5 Secured digital interfaces

The supported secure digital (SD) interface standards and their exceptions are listed here.

Table 3-18 Supported SD standards and exceptions

Applicable standard	Feature exceptions
MultiMediaCard Host Specification version 5.1	None
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

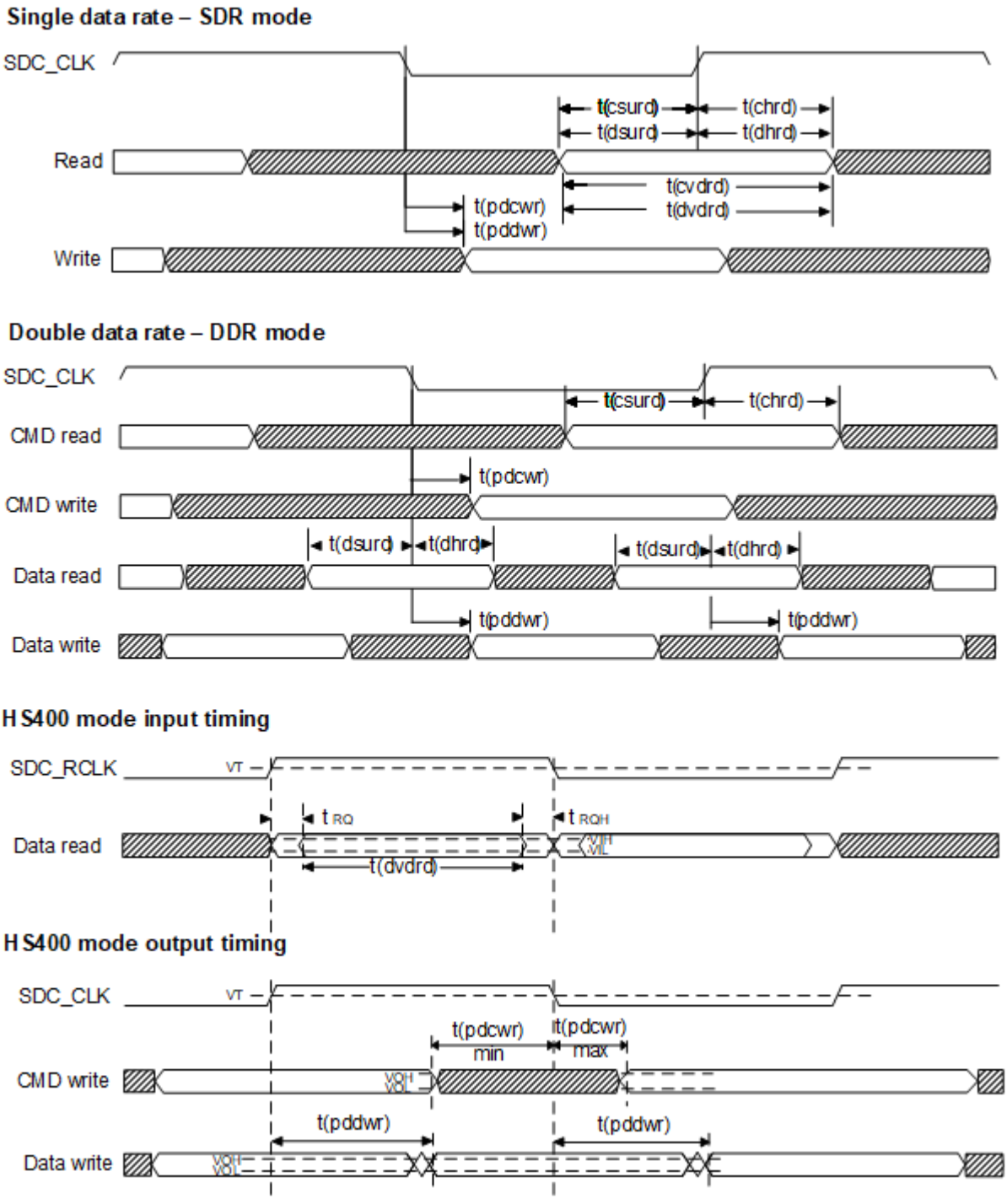


Figure 3-4 Secured digital interface timing

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3.9.6 Octa-SPI/Quad-SPI interface

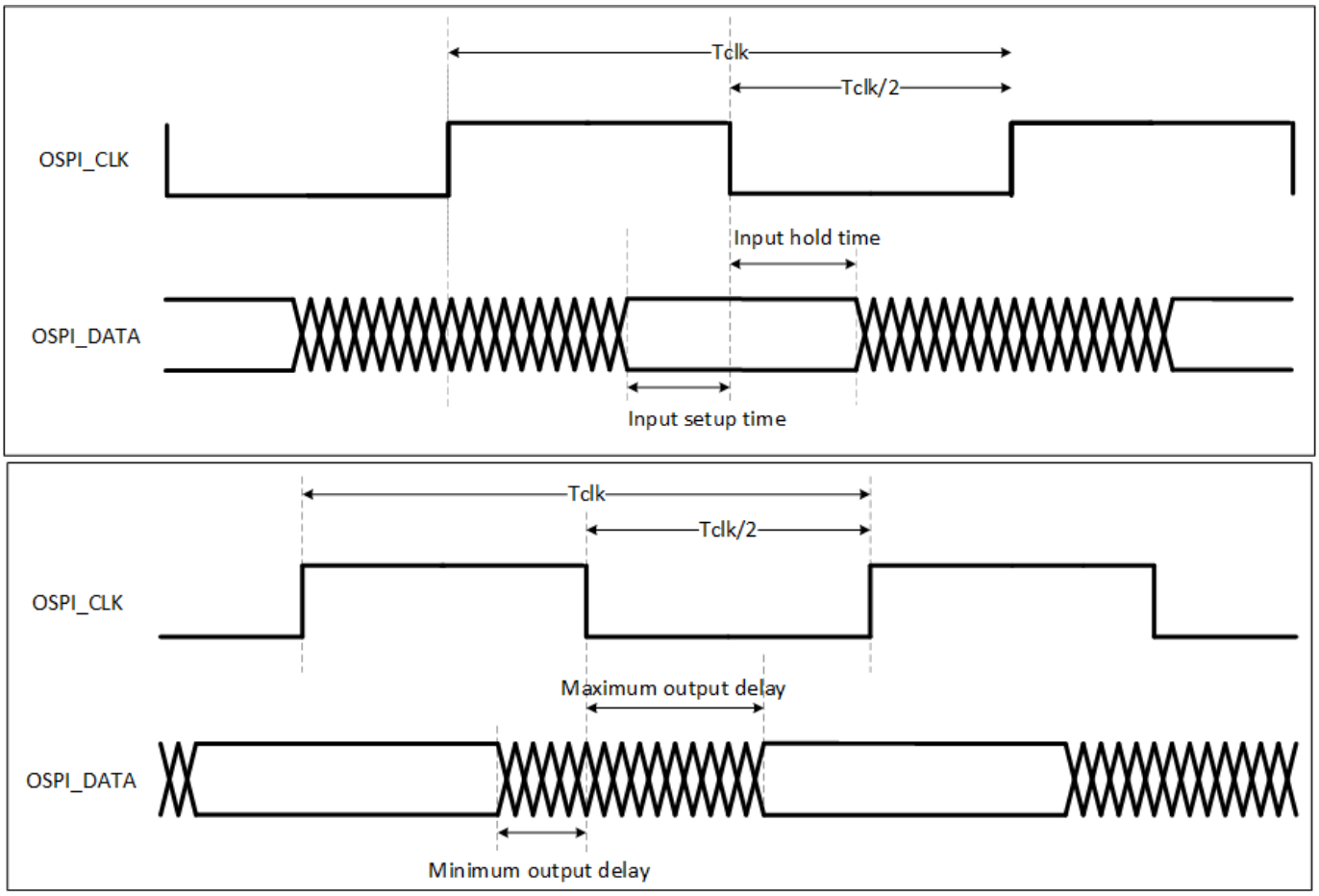


Figure 3-5 Octa-SPI/Quad-SPI SDR timing diagram

Table 3-19 Octa-SPI/Quad-SPI interface SDR timing

Parameter	Comments	Min.	Max.	Unit
1/T	OSPI/QSPI clock frequency	–	90	MHz
t(mis)	Master input setup time	1.7	–	ns
t(mih)	Master input hold time	1.3	–	ns
t(mod)	Master output delay	-2.00	2.00	ns

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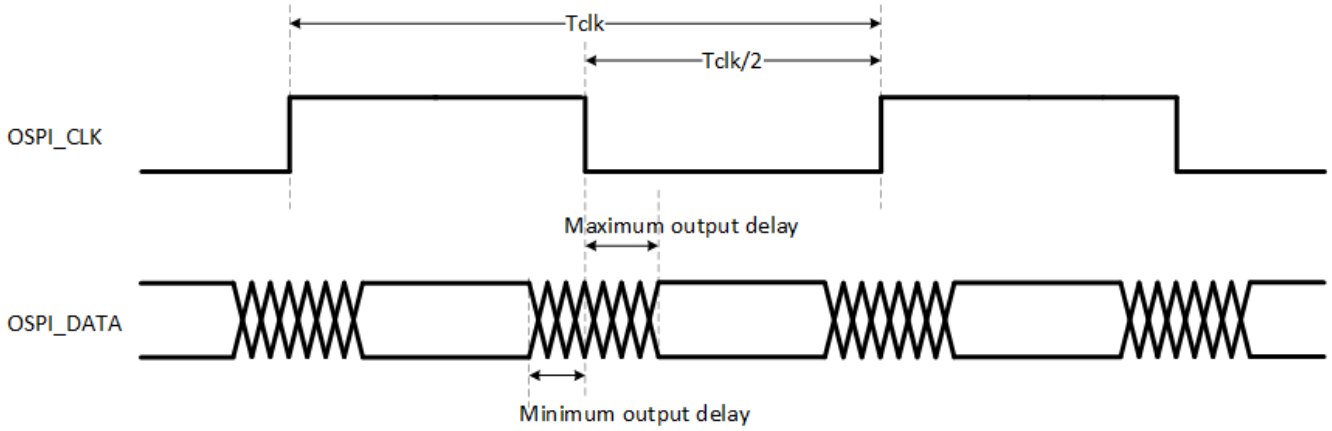


Figure 3-6 Octa-SPI DDR timing diagram

Table 3-20 Octa-SPI interface DDR timing

Parameter	Comments	Min.	Max.	Unit
1/T	OSPI clock frequency	–	166	MHz
t(skew)	DQ to DQS skew	–	530	ps
t(mod)	Master output delay	-2.00	2.00	ns

NOTE DDR is not supported on Quad-SPI operation.

3.9.7 RGMII interface

Table 3-21 Supported RGMII standards and exceptions

Applicable standard	Feature exceptions
Reduced Gigabit Media Independent Interface (RGMII) v1.3 and v2.0	None

3.9.8 I²S interfaces

Table 3-22 Supported I²S standards and exceptions

Applicable standards	Feature exceptions
Philips I²S Bus Specifications revised June 5, 1996	None

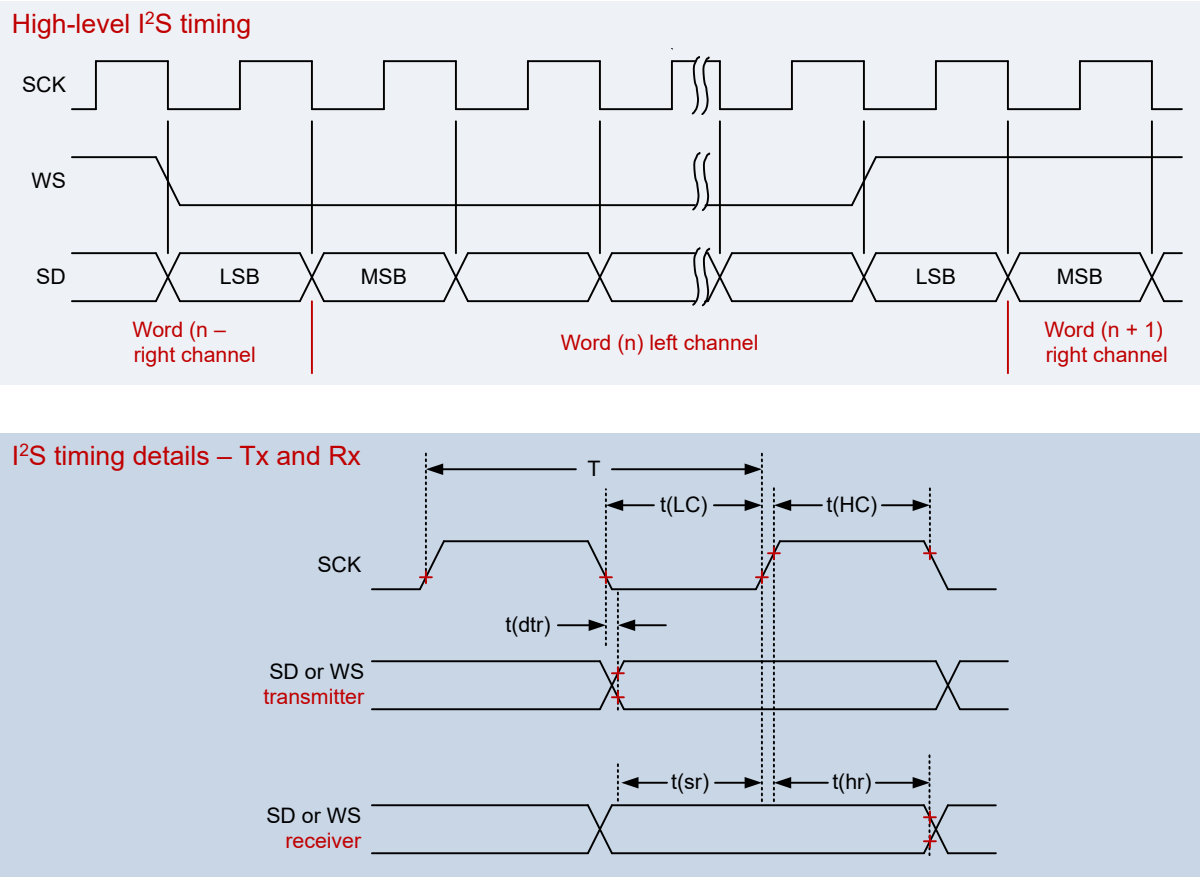


Figure 3-7 I²S timing diagram

Table 3-23 I²S interface timing

Parameter		Comments [a]	Min	Typ	Max	Unit
Using internal SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	8.14	ns
Using external SCK						
Frequency			–	–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time		8.14	–	–	ns

Table 3-23 I²S interface timing (cont.)

Parameter		Comments [a]	Min	Typ	Max	Unit
t(hr)	SD and WS input hold time		1.5	–	–	ns
t(dtr)	SD and WS output delay		–	–	8.14	ns

[a] Load capacitance is between 10 pF and 40 pF.

Table 3-24 HS-I²S Rx interface timing

Parameter		Comments [a]	Min	Typ	Max	Unit
Using external SCK						
	Frequency			–	73.728	MHz
T	Clock period		13.56	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time		2.71	–	–	ns
t(hr)	SD and WS input hold time		1.5	–	–	ns

[a] Load capacitance is between 10 pF and 40 pF.

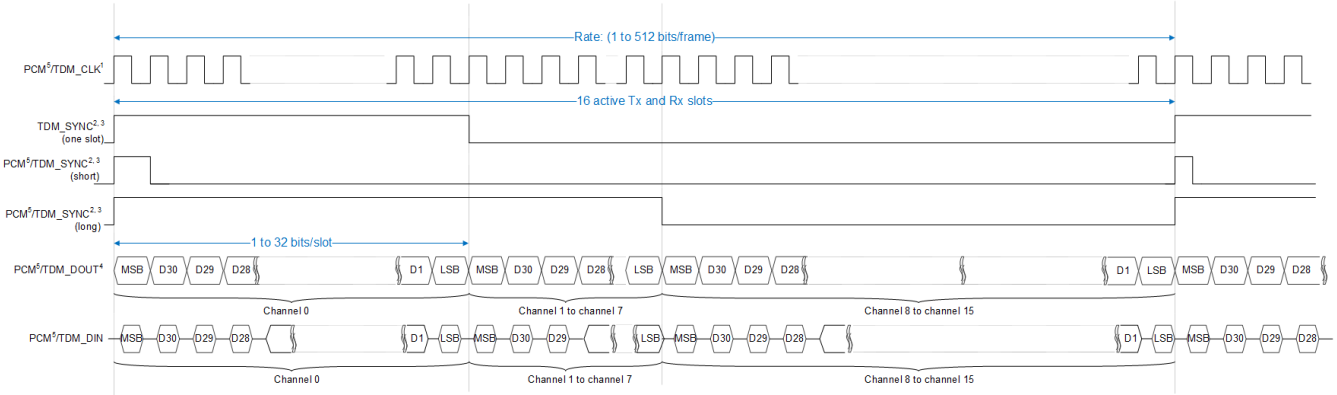
Table 3-25 HS-I²S Tx interface timing

Parameter		Comments [a]	Min	Typ	Max	Unit
Using external SCK						
	Frequency			–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(dtr)	SD and WS output delay		–	–	8.14	ns

[a] Load capacitance is between 10 pF and 40 pF.

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3.9.9 PCM/TDM interfaces



32 bits/slot; 512 bits/frame; 0 frame sync delay; 16 active Tx and Rx slots (TDM interface) or mono channel (PCM interface)

Notes:
1. Internal clock can also be inverted (180 degrees out of phase) relative to the external clock.
2. Frame sync signal can also be inverted.
3. Supports 0 to 2 cycle delays between the frame sync pulse edge and PCM_DOUT/DIN data.
4. PCM data per slot can be smaller or equal to the slot size:
   - If data size < slot size, remaining data bits are padded with zeroes.
   - If data size > slot size, extra data bits will be ignored.
5. PCM audio interface:
   - Supports only mono channel.
   - Does not support one-slot mode.
   - PCM_SYNC period is equivalent to 1 frame.

Figure 3-8 PCM/TDM audio format with different sync modes

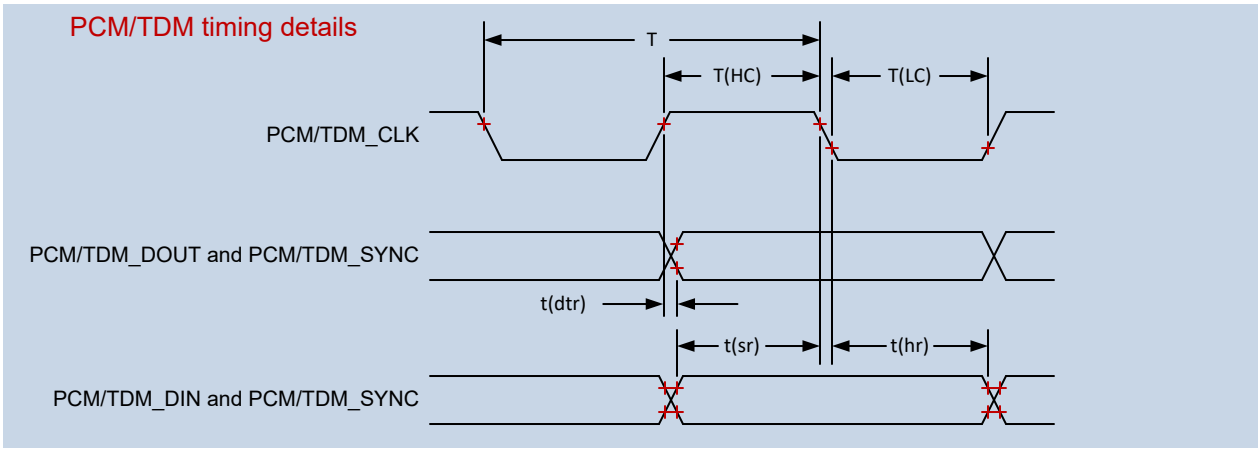


Figure 3-9 PCM/TDM timing diagram

Table 3-26 PCM/TDM interface timing parameters

Parameter		Comments	Min	Max	Unit
Master mode					
Frequency			–	24.576	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.45× T	0.55× T	ns
t(LC)	Clock low		0.45× T	0.55× T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		1.5	–	ns

Table 3-26 PCM/TDM interface timing parameters (cont.)

Parameter		Comments	Min	Max	Unit
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	8.14	ns
Slave mode					
Frequency			–	24.576	MHz
T	Clock period		40.69	–	ns
t(HC)	Clock high		0.45× T	0.55× T	ns
t(LC)	Clock low		0.45× T	0.55× T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		8.14	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		1.5	–	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC output delay		–	8.14	ns

[a] Load capacitance is between 10 pF to 40 pF.

Table 3-27 High speed PCM/TDM Rx interface timing

Parameter		Comments [a]	Min	Typ	Max	Unit
Using external SCK						
	Frequency			–	73.728	MHz
T	Clock period		13.56	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(sr)	PCM/TDM_DIN and PCM/TDM_SYNC setup time		2.71	–	–	ns
t(hr)	PCM/TDM_DIN and PCM/TDM_SYNC hold time		1.5	–	–	ns

[a] Load capacitance is between 10 pF and 40 pF.

Table 3-28 High speed PCM/TDM Tx interface timing

Parameter		Comments [a]	Min	Typ	Max	Unit
Using external SCK						
	Frequency			–	24.576	MHz
T	Clock period		40.69	–	–	ns
t(HC)	Clock high		0.45 × T	–	0.55 × T	ns
t(LC)	Clock low		0.45 × T	–	0.55 × T	ns
t(dtr)	PCM/TDM_DOUT and PCM/TDM_SYNC delay		–	–	8.14	ns

[a] Load capacitance is between 10 pF and 40 pF.

3.9.10 I²C interface

Table 3-29 Supported I²C standards and exceptions

Applicable standard	Feature exceptions
I²C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.

3.9.11 Serial peripheral interface

The QCS9075 supports SPI as a master on 25 QUP ports. SPI slave mode is supported on the eight QUP ports. See *QCS9075 Pin Assignment and GPIO Configuration Spreadsheet* (80-73417-1A) for more details.

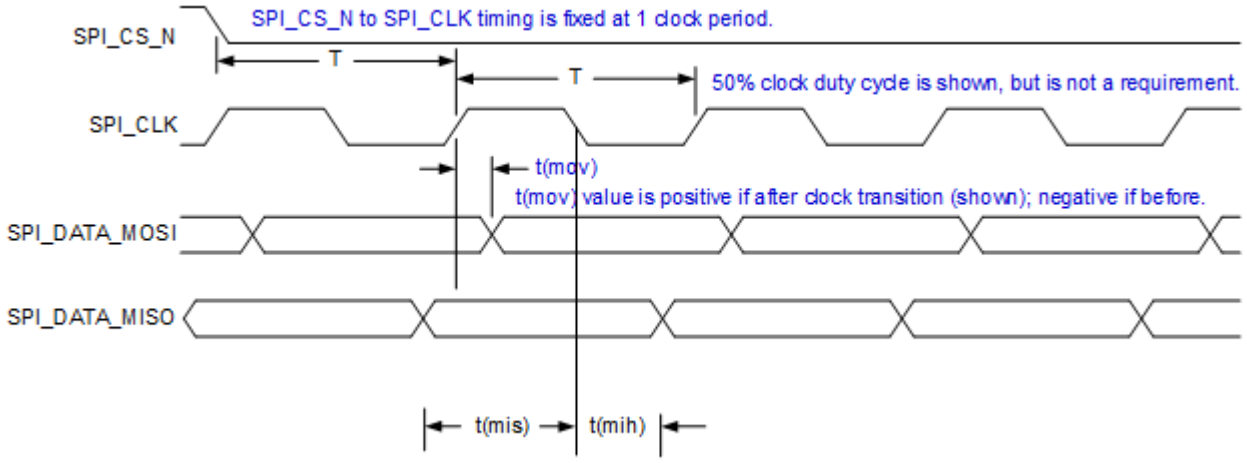


Figure 3-10 SPI master timing diagram

NOTE Depending on the mode configuration (Clock PHA and POL settings), Tx and Rx sampling edge could differ. The timing diagram above is using mode 1 as an example

Table 3-30 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T(SPI clock period) [a]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	8	–	–	ns
t(cl)	Clock low	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

[a] The minimum clock period includes 1% jitter of maximum frequency.

Table 3-31 SPI slave timing characteristics

Parameter	Comments	Min	Max	Unit
T (SPI clock period) [a]	50 MHz maximum	20.0	–	ns
t(ch)	Clock high	9	–	ns
t(cl)	Clock low	9	–	ns
t(sov)	Slave output valid	2	13	ns
t(mis)	Slave input setup	3	–	ns
t(mih)	Slave input hold	3	–	ns
S_TRI_STATE_EN [a]	Slave tri-state enable	–	14	ns
S_TRI_STATE_DIS [a]	Slave tri-state disable	–	14	ns

[a] The total capacitive load must not exceed 30 pF for a single slave system. For each additional slave, 10 pF should be added to the clock and data lines (not needed for chip select since it is one-to-one). For example, 40 pF for two slaves, although

most systems have only a single slave. Care must be taken to verify that every slave can drive the data line fast enough to meet the timing requirement or the system must use a reduced frequency.

NOTE Only SPI slave mode 1 (PHA = 1 and POL = 0) is supported.

3.9.12 CAN-FD-interface

Table 3-32 Supported CAN-FD standrads and exceptions

Applicable standard	Feature exception
ISO 11898-1: 2015, Road vehicles, Controller area network (CAN)	None
ISO 11898-4, Road vehicles, Controller area network (CAN)	None

3.10 Internal functions

Some internal functions require external interfaces to enable their operation. These include modes and resets, and JTAG functions.

3.10.1 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Digital logic characteristics.

3.10.2 JTAG

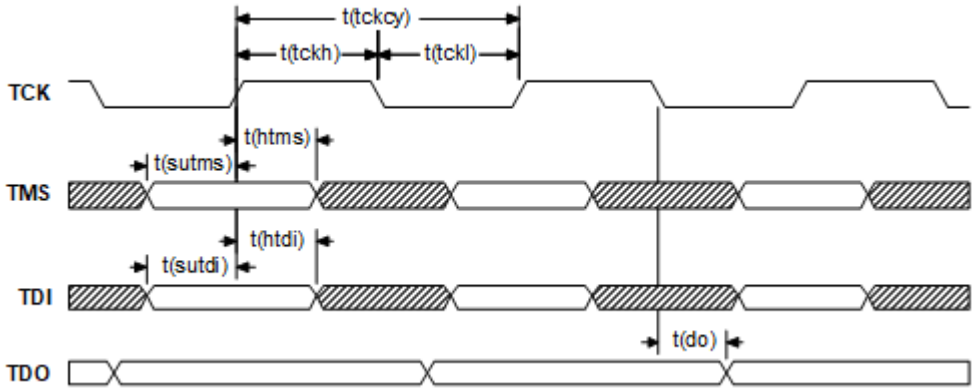


Figure 3-11 JTAG interface timing diagram

Table 3-33 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns

Table 3-33 JTAG interface timing characteristics (cont.)

Parameter		Min	Typ	Max	Unit
t(do)	TDO data output delay	–	–	15	ns
t(tckcy)	TCK period	50	–	–	ns

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4 Mechanical information

4.1 Device physical dimensions

The QCS9075 device is available in the FCBGA1723+HS package, with a 25.0 mm × 25.0 mm body and a maximum height of 2.31 mm. This package includes many ground pins for improved electrical grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. The following figure shows a simplified version of the package outline drawing.

Click *Package Outline Drawing, FCBGA1723+HS, 25.0 × 25.0 × 2.31 mm, L1250, PL1, HS1* (NT90-11744-1) to download the drawing.

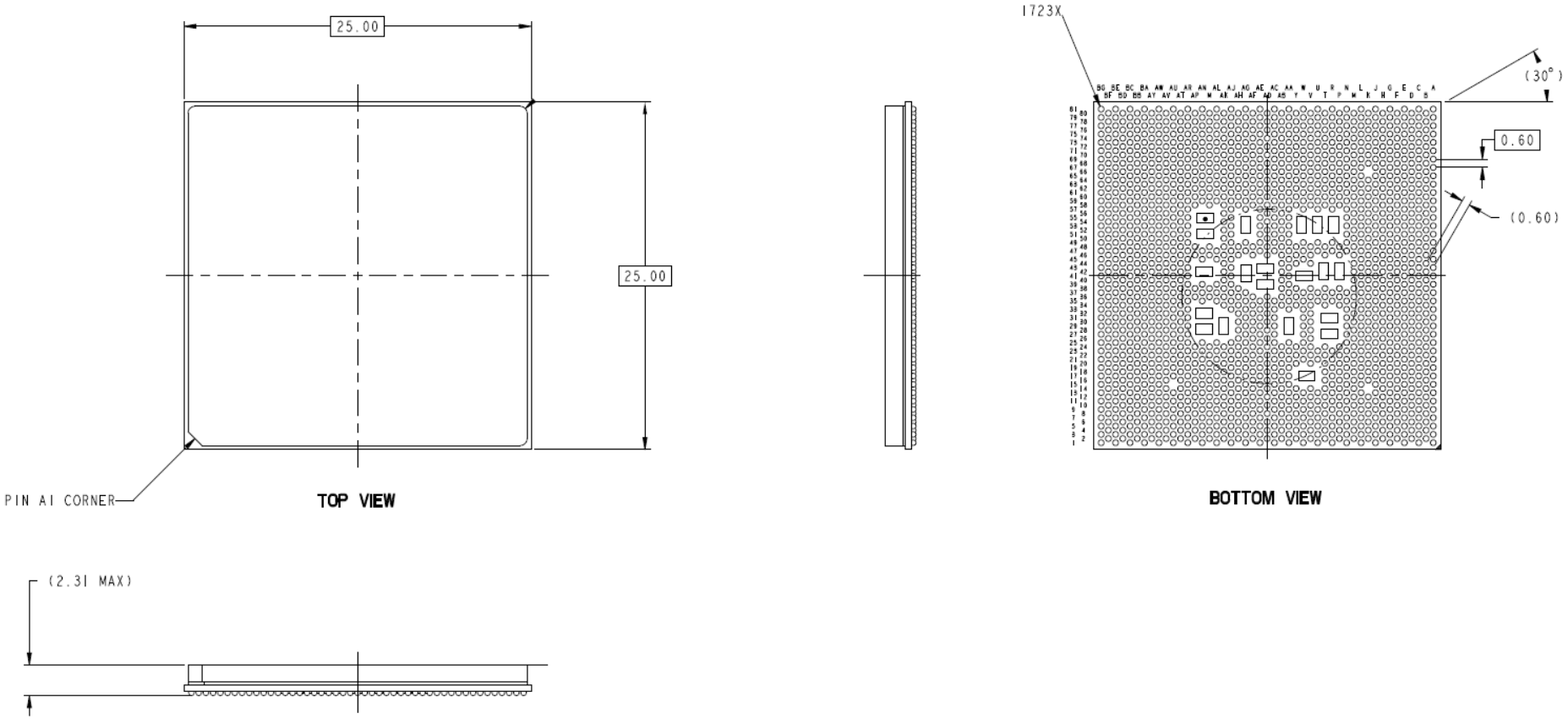


Figure 4-1 Simplified FCBGA1723+HS outline drawing

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4.2 Part marking

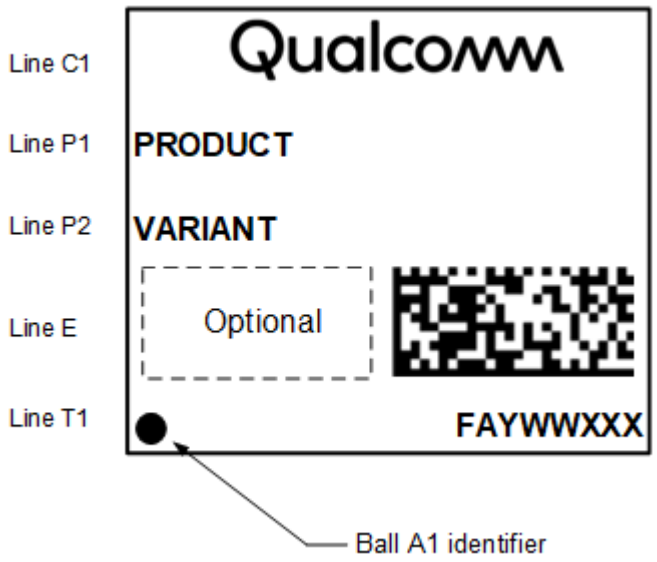


Figure 4-2 Device marking (top view, not to scale)

Table 4-1 QCS9075 marking line definitions

Line	Marking	Definition
C1	Qualcomm	Qualcomm name or logo
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ▪ QCS9075
P2	VARIANT	Device variant information ▪ See Table 4-4 for assigned values
E	Blank or random	Optional or Additional trace information
T1	•	Pin 1 or pin A1 indicator
	FAYWWXXX	F = supply source code ▪ F = J (Samsung) A = assembly site code ▪ A = C (Amkor, Korea) ▪ A = K (SPIL, Taiwan) Y = single/last digit of year WW = two-digit work week of year specified by Y XXX = traceability number

Table 4-2 QFPROM_CORR_PTE_ROW0_LSB (Address: 0x784158)

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants (see Table 4-4).
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number (see Table 4-4).

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4.3 Device ordering information

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part. This device can be ordered using the identification code shown in the following table.

Table 4-3 Example device identification code

Device ID code	AAA-AAAA	-P	TTTTTT	NNNN	A	+FF	-EE	-RR	-S [a]	-BB or -PID [b]
Symbol definition	**Product name**	**Configuration code**	**Package type**	**Number of pins**	**Package variable**	**Additional package information**	**Shipping package**	**Product revision**	**Source code**	**Feature code**
Example	QCS-9075	0	-FCBGA	1723		+HS	-TR	-00	-0	-AA

[a] Source code is always '0'
[b] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example: QCS-9075-0-FCBGA1723+HS-TR-00-0-AA.

NOTE The shipping package can be either TR (tape and reel) or MT (matrix tray).

Device identification details for all samples available to date are summarized in Table 4-4.

For availability and information about daisy chain parts, contact the Qualcomm Sales team for support.

4.4 Device identification for each sample type

Device identification details for all samples available to date are summarized in the following table.

Table 4-4 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code (if applicable) [a]	Hardware revision number	FEATURE_ID [b]	Hardware version	Source configuration code (S) [c]	Number of HTPs	Comments
QCS9075	ES	000-AA	0x1 02EB 0E1	0x0	v2.0	0	1	QCS9075, FCBGA1723+HS; Octa-core Kryo Gen6, Adreno 663 GPU, Hexagon Tensor Processor

[a] BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
[b] FEATURE_ID combined with hardware revision number defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.
[c] S is the source configuration code that identifies all the qualified die fabrication-source/assembly site combinations available when the particular sample type was shipped.

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4.5 Device moisture sensitivity level

Non-hermetically sealed packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in the following table.

Table 4-5 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85%RH
2	1 year	≤ 30°C/60%RH
2a	4 weeks	≤ 30°C/60%RH
3	**168 hours**	**≤ 30°C/60%RH, QCS9075 rating**
4	72 hours	≤ 30°C/60%RH
5	48 hours	≤ 30°C/60%RH
5a	24 hours	≤ 30°C/60%RH
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.	≤ 30°C/60%RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivityqualification. ***The QCS9075 devices are MSL3; the qualification temperature was 245°C.***

4.6 Thermal characteristics

Rather than provide thermal resistance values Θ_{JC} and Θ_{JA}, validated thermal package models are provided through the Qualcomm website. Designers can extract thermal resistance values by conducting their own thermal simulations.

Click *QCS9075 Package Thermal Models Icepak* (HS11-73417-5HW) and *QCS9075 Package Thermal Model FloTHERM* (HS11-73417-6HW) to download the thermal package models.

4.7 Package loading during heat sink attachment

The following table specifies the maximum static load for each individual component:

Table 4-6 Maximum loading specification

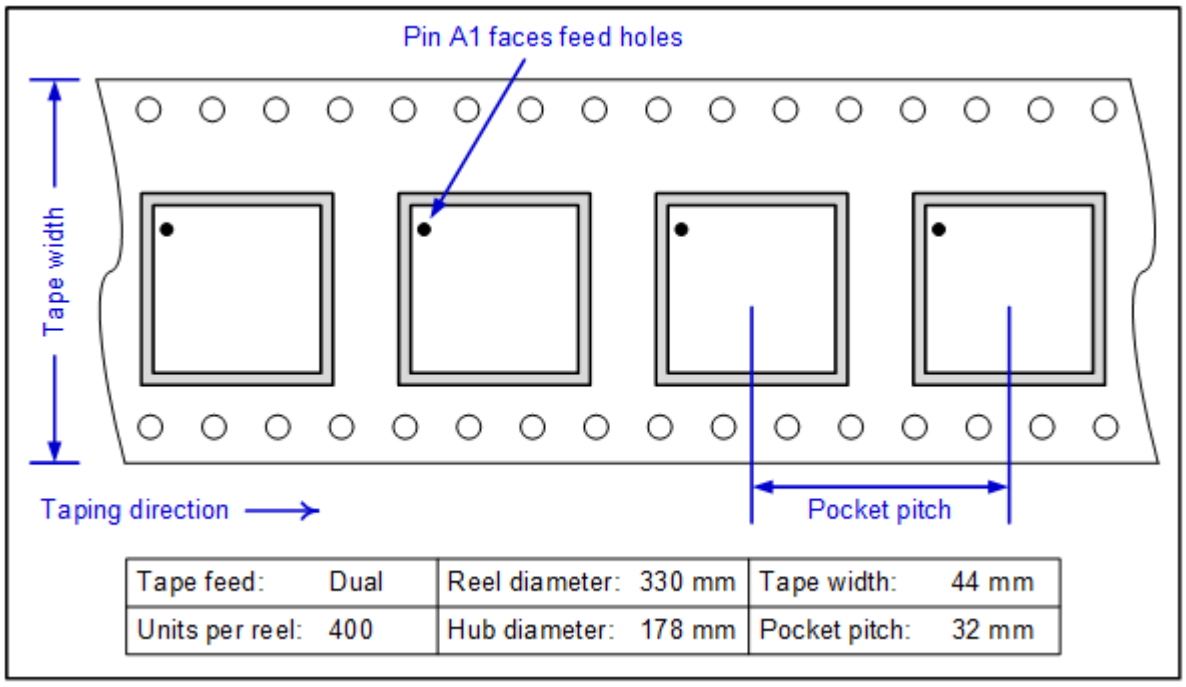
Component	Loading
QCS9075	89.6 N

The specification above will be validated through limited compressive testing with uniform loading applied perpendicular to the component surface of the packages at 125°C up to 2000 hours. It was determined that the above load recommendation is within safe working limits to ensure negligible solder ball collapse and BGA shorting risk. The end user is encouraged to validate the acceptable loading range based on intended application, motherboard, and heat sink attach configurations.

5 Carrier, handling, and storage information

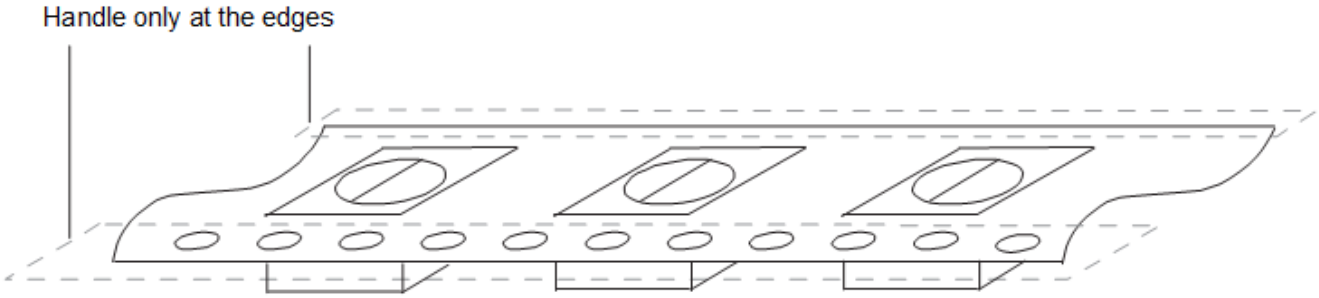
5.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards. A simplified sketch of the QCS9075 tape carrier is shown in the following figure including the proper part orientation, maximum number of devices per reel, and key dimensions



Tape feed:	Dual	Reel diameter:	330 mm	Tape width:	44 mm
Units per reel:	400	Hub diameter:	178 mm	Pocket pitch:	32 mm

Tape-handling recommendations are shown in the following figure.



5.2 Matrix tray information

All QTI matrix tray carriers confirm to JEDEC standards.

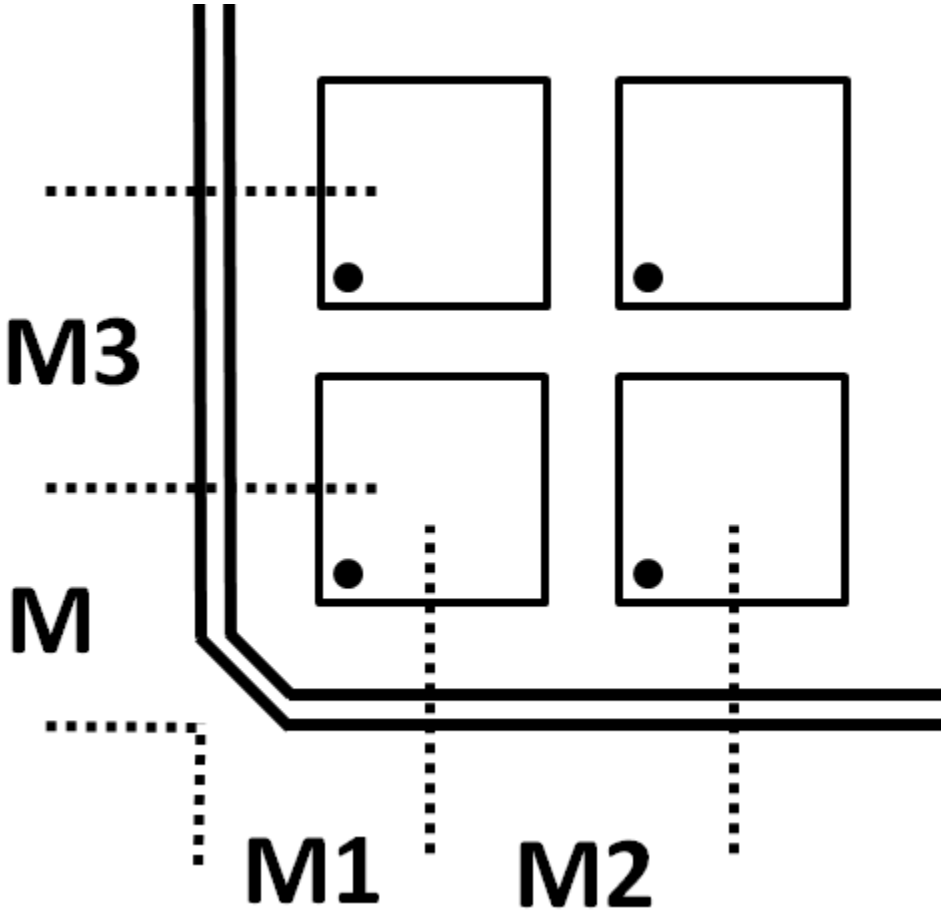
The device pin 1 is oriented to the chamfered corner of the matrix tray.

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All matrix tray media is available for sampling only. Production is supported on tape and reel.

Table 5-1 Matrix tray approved sources of supply

Key dimensions (mm)	
Array	4 × 11 (44)
M	26.70
M1	20.00
M2	27.50
M3	27.50



5.3 Storage

5.3.1 Bagged storage conditions

QCS9075 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. See *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.3.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.5

5.4 Handling

Tape handling was described in Section 5.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.4.1 Baking

It is not necessary to bake the QCS9075 if the conditions specified in Section 5.3.1 and Section 5.3.2 have not been exceeded.

It is necessary to bake the QCS9075 if any condition specified in Section 5.3.1 or Section 5.3.2 has been exceeded. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C for 24 hours. Devices should not be baked in tape and reel carriers at any temperature.

5.4.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD counter measures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*

See Reliability qualifications summary for the QCS9075 ESD ratings.

5.5 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 ELV and RoHS requirements

The device meets the substance restriction requirements of the EU ELV directive and the EU RoHS directive. Its SnAgCu solder balls have SAC405 composition.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the Qualcomm website.

https://docs.qualcomm.com/bundle/SM80-P0982-1/resource/SM80-P0982-1.pdf

After successfully logging on, the document is downloaded.

6.3 Board-level reliability

QTI conducts characterization tests to assess the device's board-level reliability. Board-level reliability data is available for download.

NOTE Click the following link to download the *Board Level Reliability, FCBGA1723+HS* (BR80-11744-1) from the Qualcomm website.

https://docs.qualcomm.com/bundle/BR80-11744-1/resource/BR80-11744-1.pdf

After successfully logging on, the document is downloaded.

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6.4 High temperature warpage

QTI measures package warpage across SMT reflow. High temperature warpage data is available for download.

NOTE Click the following link to download the *High Temperature Warpage*, FCBGA1723+HS (WR80-11744-1) from the Qualcomm website

.

https://docs.qualcomm.com/bundle/WR80-11744-1/resource/WR80-11744-1.pdf

After successfully logging on, the document is downloaded.

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7 Part reliability

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7.1 Reliability qualifications summary

The QCS9075 device has been qualified up to 115°C. The qualification plan is summarized in the following table.

Table 7-1 Qualification plan and results summary

Stress test	ABV	Test #	Test conditions/Pre and Post ATE (Identify temp, RH, and Bias)	Requirements		Results Fails/Total S.S	Comments
				S.S per lot	# LOTS		
Test Group A – Accelerated Environment Stress Tests							
Preconditioning	PC	A1	MSL3, 3X reflow (Pre and Post ATE at R)	77, (77)	3, (3)	0F/231, (231)	Pass SPIL, (ATK)
Preconditioning + bias HAST	BHAST	A2	130°C/85%RH for 96 hours (Pre and Post ATE at R and H)	77, (77)	3, (3)	0F/231, (231)	Pass SPIL, (ATK)
Preconditioning + unbiased HAST/temperature humidity	UHAST	A3	130°C/85%RH for 96 hours (Pre and Post ATE at R)	77, (77)	3, (3)	0F/231, (231)	Pass SPIL, (ATK)
Preconditioning + temperature cycle	TC	A4	Ta = -55°C to +125°C for 500 cycles (Pre and Post ATE at R and H)	77, (77)	3, (3)	0F/231, (231)	Pass SPIL, (ATK)
High temperature storage life	HTSL	A6	Ta = +150°C for 500 hours (Pre and Post ATE at R and H)	77, (77)	3, (3)	0F/231, (231)	Pass SPIL, (ATK)
Test Group B – Accelerated Lifetime Simulation Tests							
High temperature operating life	HTOL	B1	Ta ≥ 85°C for 1000 hours (Pre and Post ATE at R, C and H)	77	3	0F/231	
Early life failure rate	ELFR	B2	Ta ≥ 85°C for 48 hours (Pre and Post ATE at R and H)	800	3	0F/2400	
NVM endurance, data retention, and operational life	EDR	B3					No NVM memory on device
Test Group C – Package Assembly Integrity Tests							
Wire bond shear	WBS	C1					Not applicable, not a wirebonded package
Wire bond pull strength	WBPS	C2					Not applicable, not a wirebonded package
Solderability	S	C3					Not a leadframe package
Physical dimensions	PD	C4	Package outline drawing	10, (10)	3, (3)	0F/30, (30)	CPK≥1.67 SPIL, (ATK)

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Table 7-1 Qualification plan and results summary (cont.)

Stress test	ABV	Test #	Test conditions/Pre and Post ATE (Identify temp, RH, and Bias)	Requirements		Results Fails/Total S.S	Comments
				S.S per lot	# LOTS		
Solder ball shear	SBS	C5	5 balls each from a minimum of 10 devices, ≥ 500g/ball for pad opening 470 µm	10, (10)	3, (3)	0F/30, (30)	CPK≥1.67 SPIL, (ATK)
Lead integrity	LI	C6					Not a leadframe package
Test Group D – Die Fabrication Reliability Tests							
Electromigration	EM	D1					
Time dependent dielectric breakdown	TDDB	D2					
Hot carrier injection	HCI	D3					
Negative bias temperature instability	NBTI	D4					
Stress migration	SM	D5					
Test Group E – Electrical Verification Tests							
Pre- and post stress electrical test	TEST	E1					
ESD – human body model	HBM	E2	Pass target ±1kV with margin (Pre and Post ATE at R and H)	3	1	0F/3	Pass SPIL
ESD – charged device model	CDM	E3	Pass target ±150V with margin (Pre and Post ATE at R and H)	3, (3)	1, (1)	0F/3, (3)	Pass SPIL, (ATK)
Latch up	LU	E4	Ta = 115°C, current injection ±100 mA, over voltage test at 1.5 × VDD (Pre and Post ATE at R and H)	6	1	0F/6	Pass SPIL
Electrical distribution	ED	E5					Available for review
Fault grading	FG	E6					Available for review
Characterization	CHAR	E7					Available for review
Electromagnetic compatibility	EMC	E9					Not performed. System level test
Short circuit characterization	SC	E10					Not applicable. Not > 12 V or a power device
Soft error rate	SER	E11					Available for review
Test Group F – Defect Screening Tests							

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Table 7-1 Qualification plan and results summary (cont.)

Stress test	ABV	Test #	Test conditions/Pre and Post ATE (Identify temp, RH, and Bias)	Requirements		Results Fails/Total S.S	Comments
				S.S per lot	# LOTS		
Process average test	PAT	F1					Available for review
Statistical bin/yield analysis	SBA	F2					Available for review

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7.2 Device characteristics

Table 7-2 Device characteristics

Category	Definition
Device name	QCS9075
Package type	FCBGA1723+HS
Package body size	25.0 × 25.0 × 2.31 mm
Ball count	1723
Ball composition	SAC405
Fab sites	Samsung
Assembly sites	SPIL, Taiwan Amkor Technologies Korea (ATK)
Solder ball pitch	0.6 mm

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8 Samples and known issues

8.1 Sample testing

See Table 4-4 for device identification details for all available samples.

8.1.1 Engineering samples (ES)

These devices undergo limited testing and sometimes have significant feature limitations. They are suitable to assist with PCB development, to conduct board-level electrical evaluation tests, and to explore manufacturing considerations. Engineering samples should not be used for product-level qualification.

8.1.2 Commercial samples (CS)

These devices undergo full production-level testing, and meet the specifications and features described in the data sheet, except as otherwise noted in this document. They have passed devicelevel qualification. Commercial samples are suitable for performance testing, and also for product level production and qualification

8.2 Known issues

There are no known issues for QCS9075.

9 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
AA	September 2024	Initial release
AB	October 2024	■ Editorial changes throughout the document ■ Section 4.6 *Thermal characteristics*: Added FloTHERM thermal package model ■ Chapter 8 *Samples and known issues*: Added this chapter

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