Qualcomm Technologies International, Ltd.

CSRB31024 A06 LGA Automotive

Production Information Data Sheet

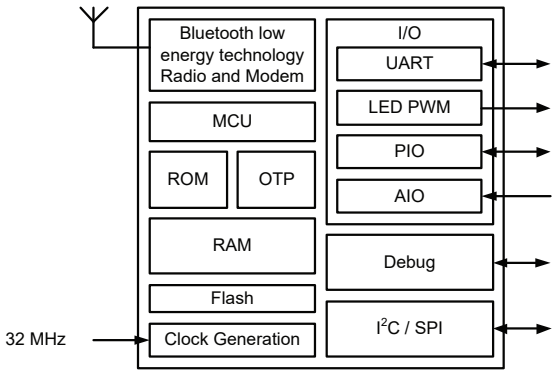
80-CU051-1 Rev. AE

November 9, 2018

Device description

- Bluetooth® low energy technology single-mode SoC
- Supported by Qualcomm® Bluetooth® Low Energy toolset and applications
- 16-bit RISC MCU, 256 KB internal SPI flash, 80 KB RAM, 192 KB ROM, 60 KB OTP
- 15 digital PIO, 1 analog AIO, SPI, I²C, quadrature decoders, LED PWM module, key scanner, 10-bit auxiliary ADC
- Ultra low-power Bluetooth low energy technology radio Bluetooth v5.0 specification compliant radio
- 36-lead 5 x 5 x 0.75 mm, 0.5 mm pitch LGA
- AEC-Q100 Automotive Grade 3 qualified

System architecture



Applications

- Bluetooth low energy technology:
  - Keyless entry system/car share
  - Infotainment remote control
  - Wireless charging controller
  - Gate/garage remote control
  - Driver health monitor
  - Driver comfort and convenience sensor/control
- Qualcomm® Mesh connectivity: Internet of Things control

General description

CSRB31024 LGA is Qualcomm Technologies International, Ltd. (QTIL)'s latest generation automotive-qualified Bluetooth low energy technology single-mode platform device with ultra low power consumption.

Qualcomm Bluetooth Low Energy technology enables ultra low-power connectivity and basic data transfer for applications previously limited by the power consumption, size constraints, and complexity of other wireless standards. The Qualcomm Bluetooth Low Energy platform provides everything required to create a Bluetooth low energy technology product with RF, baseband, MCU, qualified Bluetooth v5.0 specification stack, and customer application running on a single IC.

Bluetooth low energy technology enables connectivity and data transfer to leading smartphone, tablet, and personal computing devices including iOS, Android, Windows Phone 8, and Blackberry OS10 devices.

Qualcomm Mesh places the smartphone at the center of the Internet of Things enabling an almost unlimited number of Bluetooth low energy technology enabled devices to be simply networked together and controlled directly from a single smartphone, tablet, or PC.

CSRB31024 LGA supports profiles for advanced remote controls and custom profiles (such as keyless entry and automotive switch pack).

Device details

Ultra low-power Bluetooth low energy technology radio

- Single pin RF connection (50 Ω impedance in Tx and Rx modes)
- Requires no external RF components[a]
- Operates from a single crystal
- Bluetooth v5.0 specification compliant

Bluetooth transmitter

- 4 dBm RF transmit power
- Tx power control
- No external power amplifier or Tx/Rx switch required

Bluetooth receiver

- -90.0 dBm sensitivity
- Rx Boost mode available: Enhances Rx sensitivity at higher receive current cost
- Receiver large input level saturation -5 dBm
- Integrated channel filters
- Digital demodulator for improved sensitivity and cochannel rejection
- Fast AGC for enhanced dynamic range

Bluetooth stack

QTIL protocol stack runs on the integrated MCU:

- Support for Bluetooth v5.0 specification features:
  - Master and slave operation
  - Including encryption
- Software stack in firmware includes:
  - GAP
  - L2CAP
  - Security manager
  - Generic attribute protocol
  - Attribute profile
  - Bluetooth low energy technology profile support

Synthesizer

- Fully integrated synthesizer requires no external VCO varactor diode, resonator, or loop filter

Baseband and software

- Integrated MAC for all packet types enables packet handling without the need to involve the MCU

[a] Certain antennas with gain may require a simple filter.

Physical interfaces

- 15 digital flexible PIO
- 1 analog AIO
- UART
- SPI interface
- Debug SPI interface for programming
- I²C controller
- 4 x quadrature decoders
- 5 x LED PWMs
- Keyboard scanner
- 10-bit auxiliary ADC

Auxiliary features

- Battery monitor
- 6 power modes
- Power management features include software shutdown and hardware wake-up
- Wake-up power management from any PIO
- Integrated switch-mode power supply
- Linear regulator (internal use only)
- AES-128
- Watchdog timer

Memory

- 256 KB internal flash
- 64 KB (Code) and 16 KB (Data) RAM
- 192 KB ROM
- 60 KB OTP

Battery

- Battery input voltage 2.7 V to 3.3 V

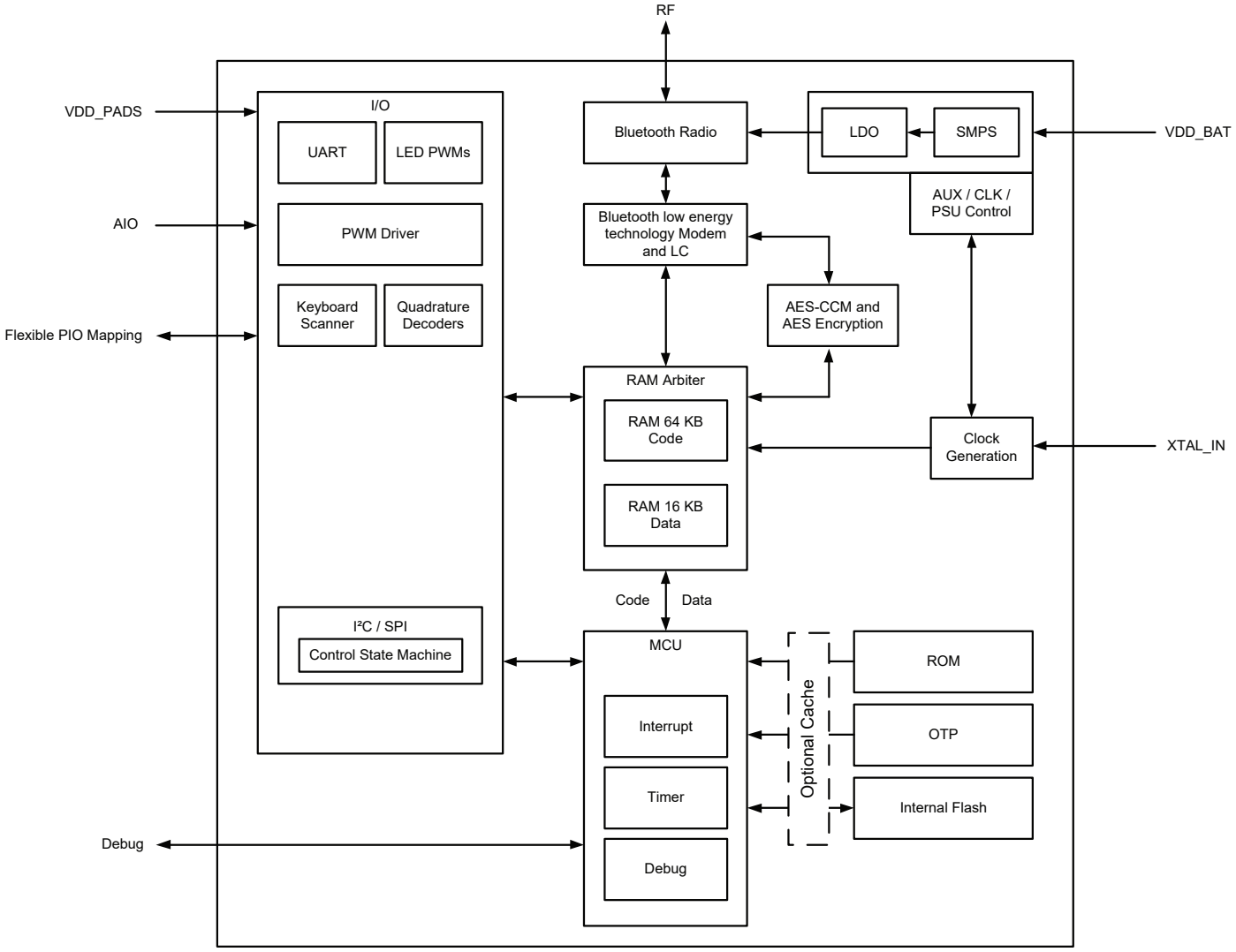
Temperature specification

- Operating temperature -40 to 85 ºC

Package

- 36-lead 5 x 5 x 0.75 mm, 0.5 mm pitch LGA
- Single side routing pinout optimized

CSRB31024 LGA functional block diagram



CSRB31024 LGA functional block diagram

Ordering information

Device	Package			Order number
	Type	Size	Shipment method	
CSRB31024 LGA	LGA 36-lead (Pb free)	5 x 5 x 0.75 mm 0.5 mm pitch	Tape and reel	CSR-B31024-0-36BLGA-MT-00-0

NOTE Your attention is drawn to QTIL's Terms of Supply, see http://www.qualcomm.com/salesterms or please request a copy), in particular the section covering Product Warranties and Disclaimers. Please note that the product warranty differs for production, pre-production, and other versions.

Production status minimum order quantity is 2 kpcs.

Supply chain: QTIL's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

QTIL contacts

General information	http://www.qualcomm.com
Information on this product	qcsales@qti.qualcomm.com
Customer support for this product	http://www.csrsupport.com
	http://createpoint.qti.qualcomm.com
Details of compliance and standards	product.compliance@qti.qualcomm.com
Help with this document	document.feedback@qti.qualcomm.com

Revision history

Revision	Date	Change reason
1	February 2017	Initial release. Alternative document number CS-00401212-DS.
AA	June 2017	Updated to Engineering Sample.
AB	October 2017	Updated to Pre-production Information.
AC	November 2017	Updated Operating Conditions.
AD	February 2018	Updated Operating Conditions.
AE	November 2018	Updated to Production Information.

Status information

QTIL Product Data Sheets progress according to the following formats: Advance Information, Engineering Sample, Pre-production Information, and Production Information. The status of this document is **Production Information**.

Advance Information

Information for designers concerning QTIL product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

Engineering Sample

Information about initial devices. Devices are untested or partially tested prototypes, their status is described in an Engineering Sample Release Note. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by QTIL without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalized. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by QTIL without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Device implementation

As the feature-set of the CSRB31024 LGA is firmware build-specific, see the relevant software release note for the exact implementation of features on the CSRB31024 LGA.

Life support policy and use in safety-critical applications

QTIL products are not authorized for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. QTIL will not warrant the use of its devices in such applications.

QTIL environmental and RoHS compliance

CSRB31024 LGA devices meet the requirements of Directive 2011/65/EU of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

CSRB31024 LGA devices are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see QTIL *Environmental declaration statement for QTIL semiconductor products*.

Contents

Tables

Figures

1 Package information

CSRB31024 LGA is available in a 5 x 5 x 0.75 mm 36-lead LGA package.

1.1 Chip marking

Chip marking identifies lot-specific information about CSRB31024 LGA.

Figure 1-1 shows the product marking for CSR-B31024-0-36BLGA-MT-00-0 in a 36-lead 5 x 5 x 0.75 mm LGA package.

bkd1538126922433.1

Figure 1-1 CSRB31024 LGA chip marking

NOTE Figure 1-1 is not to scale. The marking font and image are for illustration purposes only.

The square location mark identifies pin 1.

Table 1-1 CSRB31024 LGA chip marking content

Line	Description	Definition
1	CSR logo	-
2	Device number	B31024
3	Device number	AU
4	Manufacturing trace code	YWWXXX ■ Y: Assembly year ■ WW: Assembly week ■ XXX: Lot designator

1.2 CSRB31024 LGA pinout diagram

The CSRB31024 LGA IC has 36 leads, numbered sequentially in an anticlockwise (counterclockwise) direction, starting from lead 1.

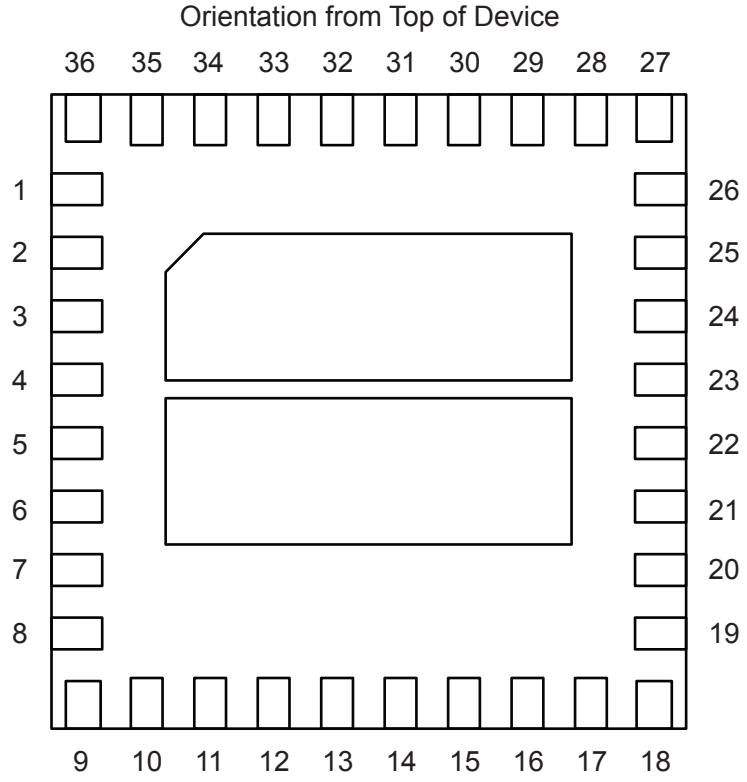


Figure 1-2 CSRB31024 LGA pinout diagram

1.3 Device terminal functions

The leads on the CSRB31024 LGA are grouped into various terminal functions. The device terminal functions include:

- Radio
- Synthesizer and oscillator
- PIO port
- Test and debug
- Power supplies and control

1.3.1 Device terminal functions (Radio)

Table 1-2 CSRB31024 LGA device terminal functions (Radio)

Radio	Lead	Pad type	Supply domain	Description
RF	3	RF	VDD_RF	Antenna port for Bluetooth transmitter / receiver.

1.3.2 Device terminal functions (Synthesizer and oscillator)

Table 1-3 CSRB31024 LGA device terminal functions (Synthesizer and oscillator)

Synthesizer and oscillator	Lead	Pad type	Supply domain	Description
XTAL_IN	6	Analog	VDD_RF	Reference clock input.
XTAL_OUT	5	Analog	VDD_RF	Drive for clock crystal.

1.3.3 Device terminal functions (PIO port)

Table 1-4 CSRB31024 LGA device terminal functions (PIO port)

PIO port	Lead	Pad type	Supply domain	Description
PIO[14]	20	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 14.
PIO[13]	1	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 13.
PIO[12]	36	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 12.
PIO[11]	35	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 11.
PIO[10]	34	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 10.
PIO[9]	33	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 9.

Table 1-4 CSRB31024 LGA device terminal functions (PIO port) (cont.)

PIO port	Lead	Pad type	Supply domain	Description
PIO[8]	32	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 8.
PIO[7]	30	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 7.
PIO[6]	29	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 6.
PIO[5]	28	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 5.
PIO[4]	27	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 4.
PIO[3]	25	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 3.
PIO[2]	24	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 2.
PIO[1]	23	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 1.
PIO[0]	22	Digital: Bidirectional with programmable strength internal pull-up / pull-down	VDD_PADS	General programmable I/O line 0.
AIO[0]	9	Unidirectional analog	VDD_AUX	Analog programmable input line.

1.3.4 Device terminal functions (Test and debug)

Table 1-5 CSRB31024 LGA device terminal functions (Test and debug)

Test and debug	Lead	Pad type	Supply domain	Description
SPI_PIO#	21	Input with strong internal pull-down	VDD_PADS	Logic high switches PIO[3:0] to Debug SPI operation, low to PIO mode.

1.3.5 Device terminal functions (Power supplies and control)

Table 1-6 CSRB31024 LGA device terminal functions (Power supplies and control)

Power Supplies and Control	Lead	Description
VDD_BAT	10	Positive supply from the battery.
SMPS_LX1	11	Terminal 1 of the external 2.2 µH inductor connected to this pin.
SMPS_LX2	12	Terminal 2 of the external 2.2 µH inductor connected to this pin.
VDD_AUX	15	SMPS output for the auxiliary rail and AIO port.
VDD_DIG	16	SMPS output for the digital rail.
VDD_MEM	17	SMPS output for the memory rail.
VDD_RAD	13	SMPS output for the radio rail.
VDD_RF_IN	14	SMPS output for the radio rail.

Table 1-6 CSRB31024 LGA device terminal functions (Power supplies and control) (cont.)

Power Supplies and Control	Lead	Description
VDD_RF	7	Decoupled supply for radio and XTAL pads.
VSS_RF	4, 2	Ground connection for RF.
VDD_PADS	26, 19	Positive supply for digital I/O ports PIO[14:0] and SPI_PIO#.
VSS	31, 18, 8 and the central pads	Ground connections.

1.4 Package dimensions

CSRB31024 LGA is available in a 5 x 5 x 0.75 mm 36-lead LGA package.

Package dimensions diagram

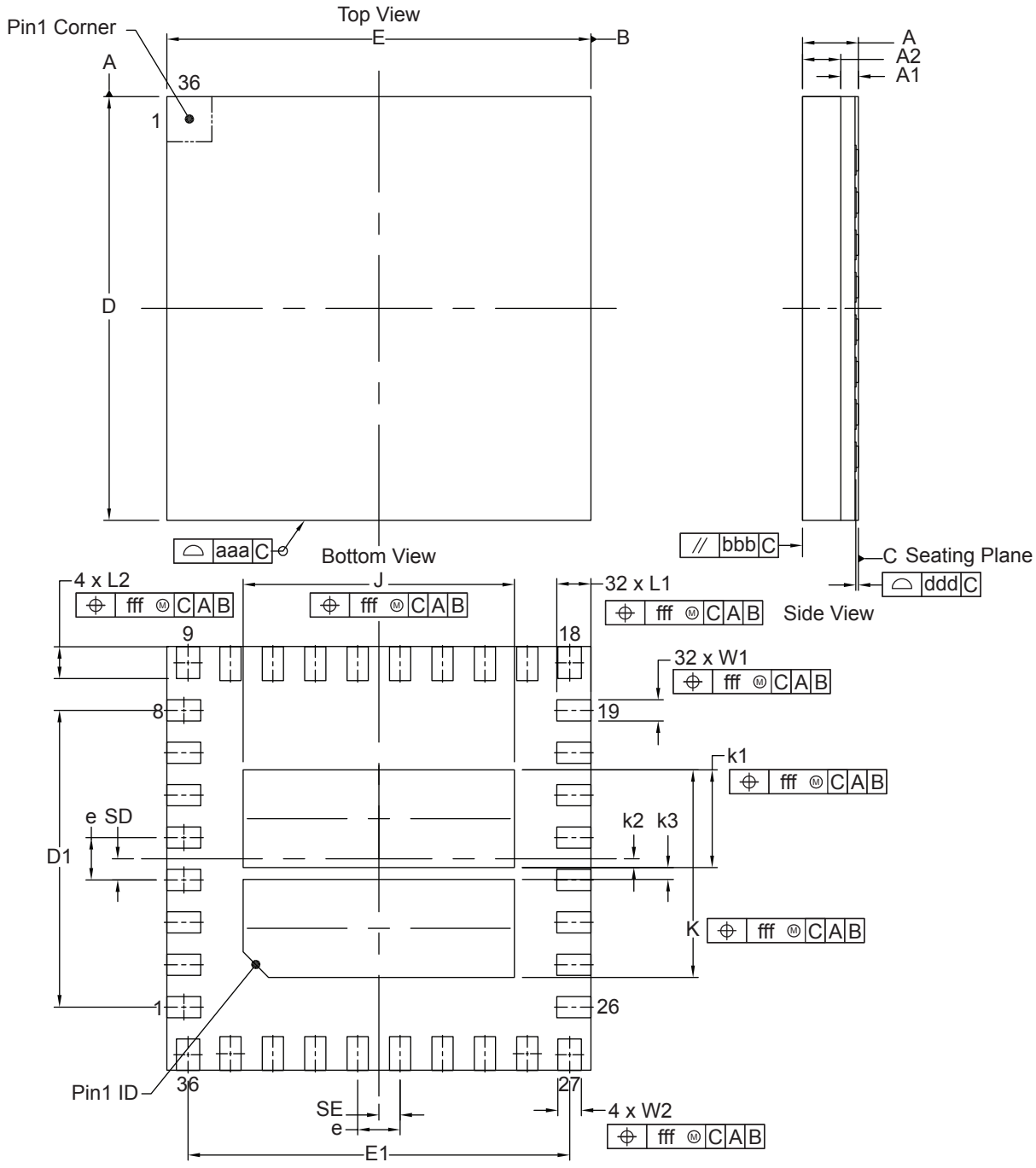


Figure 1-3 CSRB31024 LGA package dimensions diagram

Package dimensions table

Table 1-7 CSRB31024 LGA package dimensions table

Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	-	0.66	0.75	k2	-	0.105	-
A1	-	0.21	-	k3	-	0.140	-
A2	-	0.45	-	L1	0.35	0.4	0.45
D and E	4.9	5.0	5.1	L2	0.325	0.375	0.425
D1	-	3.5	-	SD and SE	-	0.25	-
E1	-	4.5	-	W1	0.2	0.25	0.3
e	-	0.5	-	W2	0.225	0.275	0.325
J	3.15	3.20	3.25	aaa, bbb, fff	-	0.1	-
K	2.40	2.45	2.50	ddd	-	0.08	-
k1	1.105	1.155	1.205	-	-	-	-
Notes	1. Dimensioning and tolerances conform to ASME Y14.5M. - 1994. 2. Pin #1 identifier is placed on the top surface of the package. Exact shape and size of this feature is optional. 3. Parallelism measurement excludes any effect of marks on the top surface of the package. 4. The 4 leads (9, 18, 27 and 36) are wider and shorter than all other leads.						
Description	36-lead Land Grid Array Package						
Size	5 x 5 x 0.75 mm			**JEDEC**	N/A		
Pitch	0.5			**Units**	mm		

1.5 PCB design and assembly considerations

This section lists recommendations to achieve maximum board-level reliability of the 5 x 5 x 0.75 mm LGA 36-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- QTIL recommends that the PCB land pattern is in accordance with IPC standard IPC-7351.
- Solder paste must be used during the assembly process.

1.6 Typical solder reflow profile

For information, see *Typical Solder Reflow Profile for Lead-free Devices Information Note* (80-CT462-1).

2 Bluetooth modem

CSRB31024 LGA's modem supports Bluetooth low energy technology and has four link controller blocks supporting up to four connections.

2.1 RF port

CSRB31024 LGA contains a single-ended 50 Ω RF Tx / Rx port pin. No external matching to 50 Ω is required.

NOTE The antenna must be connected when CSRB31024 LGA is powered up. Significant changes in VSWR after the chip has performed start of day calibrations might result in Tx modulation errors and reduced Rx sensitivity.

2.2 RF receiver

The receiver features a near-zero IF architecture enabling the channel filters to be integrated onto the die. Sufficient out-of-band blocking provided on die at the LNA input enables the receiver to be used close to cellular phone transmitters without being significantly desensitized:

- Receive sensitivity is typically-90.0 dBm
- Software selectable Boost mode can be enabled for extra sensitivity
- An AGC supports the device to meet Bluetooth v5.0 specification
- Receiver large input level saturation is typically -5 dBm

NOTE CSRB31024 LGA does not support control for an external LNA. The additional front-end gain from an LNA would compromise the Bluetooth maximum input signal level test RCV-LE/CA/BV-06-C.

2.2.1 RSSI

Front-end LNA gain is changed according to measured RSSI, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference-limited environments. The level is reported to the firmware using an API with accuracy of ±6 dBm, and resolution of 1 dBm.

NOTE This value is only available to an application after reception of a valid packet.

2.3 RF transmitter

2.3.1 Power amplifier

The internal PA can deliver a maximum of 4 dBm at the RF pin into a 50 Ω load. Configurable software enables delivery of lower output powers to reduce current consumption during transmit.

2.4 Bluetooth radio synthesizer

The Bluetooth radio synthesizer is fully integrated onto the die with no requirement for external components and meets all lock-time requirements of the Bluetooth v5.0 specification.

2.5 Baseband

2.5.1 Physical layer hardware engine

Dedicated logic performs:

- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation

3 Clock generation

3.1 Clock architecture

Figure 3-1 shows CSRB31024 LGA's three clocks:

- Fast Clock:
  - Bluetooth system reference clock required for Tx and Rx
  - Supplied by an external 32 MHz crystal
- Intermediate Clock:
  - Internal clock source that can operate at various intermediate frequencies (62.5 kHz to 8 MHz in approximate log spacing)
  - Suitable for peripherals that require a moderate clock frequency of low accuracy
  - Lower power than Fast Clock and can work in Deep Sleep
- Slow Clock:
  - Internal clock source
  - Lowest power and works in Deep Sleep
  - A digital state machine uses temperature sampling to ensure clock drift for sleep timing stays within 500 ppm
  - Internally generated, running at approximately 32 kHz, without trim, only calibration

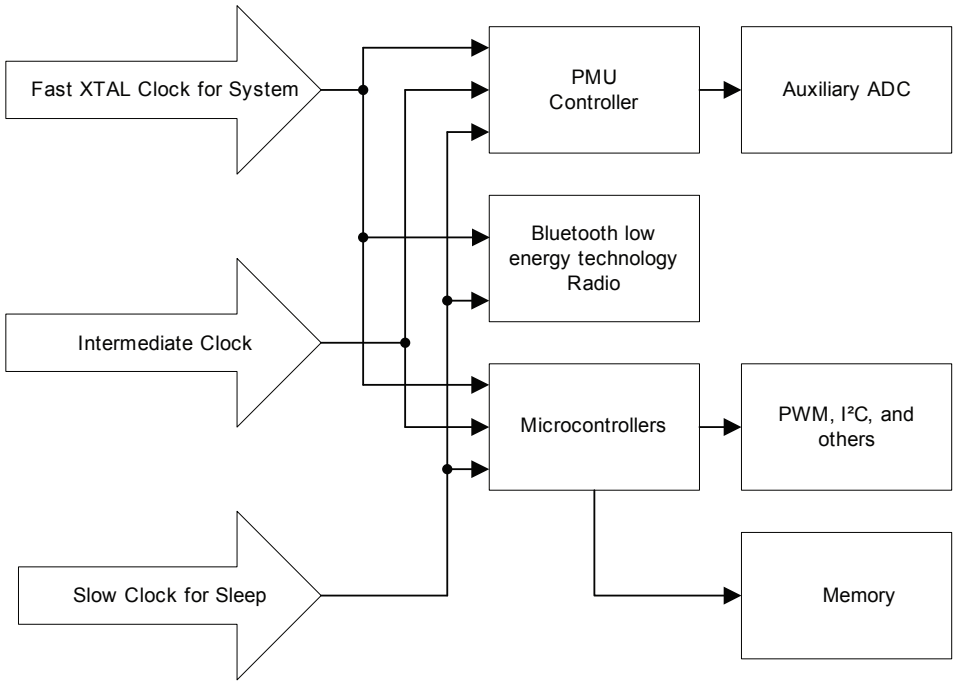
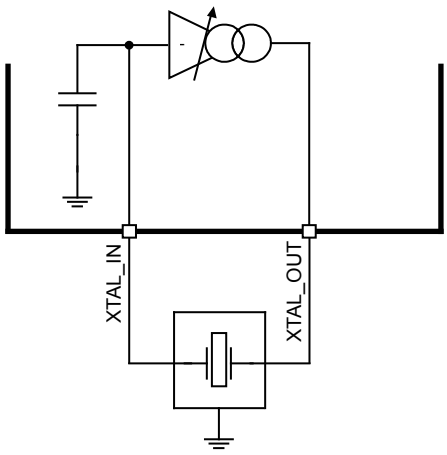


Figure 3-1 CSRB31024 LGA clock architecture

3.2 Crystal oscillator: XTAL_IN and XTAL_OUT

CSRB31024 LGA has a crystal driver circuit. This operates with an external crystal to form a Pierce oscillator. Figure 3-2 shows how the external crystal is connected to pins XTAL_IN and XTAL_OUT.

NOTE The crystal oscillator requires no external capacitors.



spb1480083203577.2

Figure 3-2 Crystal driver circuit

NOTE The PCB design must ensure that the total trace capacitance on XTAL_IN and XTAL_OUT are less than 2 pF each.

3.2.1 Crystal specification

Table 3-1 lists the specification required for a CSRB31024 LGA external crystal.

NOTE Crystals with the specification in Table 3-1 are produced by a limited number of manufacturers. QTIL recommends only using crystals listed in *CSR102x Recommended Crystals Specification*.

Table 3-1 Crystal specification

Parameter	Description	Min	Typ	Max	Unit
F_{nom}	Nominal fundamental frequency	-	32	-	MHz
T_{stg}	Storage temperature	-40	-	125	°C
$T_{op\_automotive}$	Operating Temperature range	-40	-	85	°C
C_P	Package capacitance (32 MHz)	-	0.8	-	pF
C_L	Load capacitance	-	6	-	pF
F_tol_nom	Frequency Tolerance nominal at room temperature	-10	-	10	ppm
F_tol_temp_auto [a]	Frequency stability over temperature (automotive)	-20	-	20	ppm
F_tol_aging	Frequency tolerance aging 1st year @ 25°C	-3	-	3	ppm/yr
Sensitivity	Frequency variation vs. load capacitance changes @ 25°C	-	30	40	ppm/pF
ESR	Motional Resistance (32 MHz)	-	20	60	Ω

[a] Wider temperature range (than industrial) requires a wider ppm tolerance

3.2.2 Crystal configuration

The crystal must be configured on each device during the manufacturing process.

NOTE For information about crystal configuration, see *CSR102x Initial Configuration for Devices* (80-CF263-1) (part of Qualcomm Bluetooth Low Energy SDK).

3.3 Sleep clock

CSRB31024 LGA uses the internal slow clock or crystal in low-power mode, eliminating the need for an externally supplied sleep clock.

4 Operating modes

CSRB31024 LGA has six operating modes. Four are Deep Sleep modes:

- Active mode
- Radio-on mode
- Deep Sleep modes:
  - Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention mode
  - Deep Sleep: 16 KB Data RAM Retention mode
  - Deep Sleep: No RAM Retention and External Interrupts and Timer Enabled (Hibernate) mode
  - Deep Sleep: No RAM Retention and External Interrupts Enabled (Dormant) mode

4.1 Active mode

In Active mode, the processor runs:

- Code and/or performs activities with peripherals.
- With at least one link controller powered.

4.2 Radio-on mode

In Radio-on mode, the Bluetooth radio is turned on.

NOTE Radio-on mode can only be entered from Active mode.

4.3 Deep Sleep modes

CSRB31024 LGA has four Deep Sleep modes.

4.3.1 Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention mode

In Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention mode:

- Normal operation uses only the slow clock or intermediate clock (running at a slow speed).
- CSRB31024 LGA supports activity in peripherals to perform a particular operation (for example PWMs, keyboard scanner) or wake the chip on activity (for example UART, application SPI).
- Link controller state is maintained: This can be active (advertising, scanning or in a connection) and CSRB31024 LGA can deep sleep between periods on or around radio activity.
- A PIO deep sleep timer time-out or optional temperature change or low battery can wake the chip by generating an interrupt.
- It is possible to keep the processor powered and its power-controlled using power gating.

4.3.2 Deep Sleep: 16 KB Data RAM Retention mode

In Deep Sleep: 16 KB Data RAM Retention mode:

- Normal operation uses only the slow clock or intermediate clock (running at a slow speed).
- CSRB31024 LGA supports activity in peripherals to perform a particular operation (for example PWMs, keyboard scanner) or wake the chip on activity (for example UART, application SPI).
- Link controller state is maintained: This can be active (advertising, scanning or in a connection) and CSRB31024 LGA can deep sleep between periods on or around radio activity.
- A PIO deep sleep timer time-out or optional temperature change or low battery can wake the chip by generating an interrupt.
- It is possible to keep the processor powered and its power-controlled using power gating.

4.3.3 Deep Sleep: No RAM Retention and External Interrupts and Timer Enabled (Hibernate) mode

In Deep Sleep: No RAM Retention and External Interrupts and Timer Enabled (Hibernate) mode:

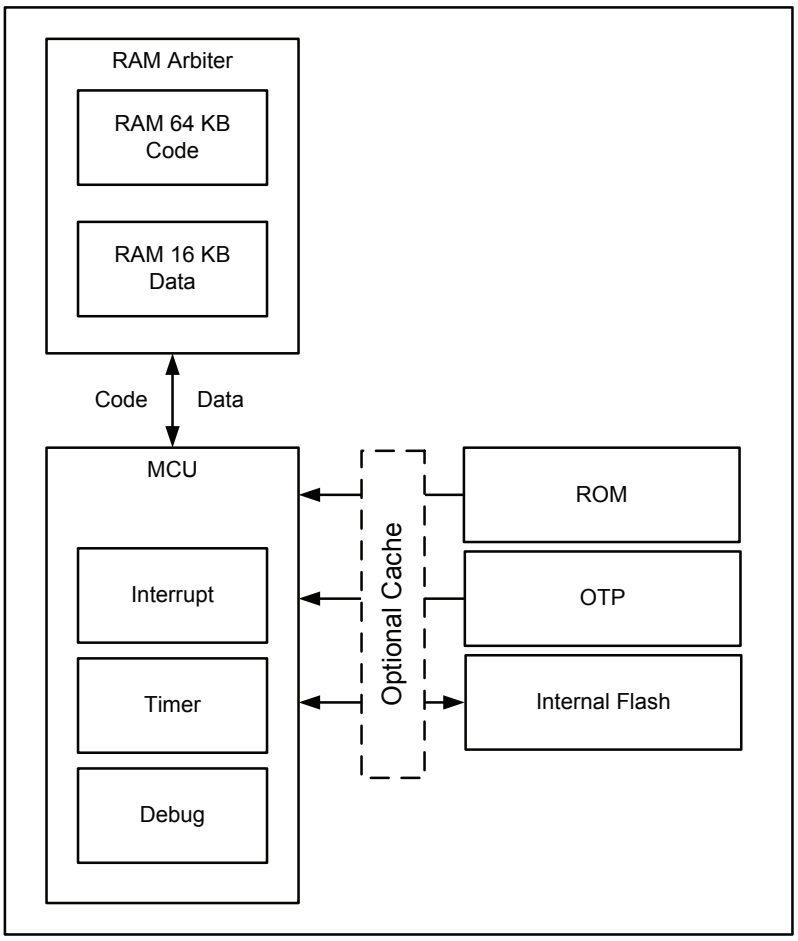
- VDD_BAT must always be present.
- A PIO can wake the chip (programmable as in Deep Sleep: No RAM Retention and External Interrupts Enabled (Dormant) mode).
- The following can wake the chip:
  - PIO hibernate timer time-out.
  - Temperature change.
  - Low battery.

4.3.4 Deep Sleep: No RAM Retention and External Interrupts Enabled (Dormant) mode

In Deep Sleep: No RAM Retention and External Interrupts Enabled (Dormant) mode:

- An attached battery can be used as a wake-up.
- No timers run, therefore CSRB31024 LGA can only be woken by a PIO or a rise on VDD_BAT.
- VDD_BAT can be removed if VDD_PADS remains powered, because the pull states of pads are preserved.
- Ignore a rise on VDD_BAT until a PIO has latched an event (enabling two different Deep Sleep: No RAM Retention and External Interrupts Enabled submodes).
- The PIOs that CSRB31024 LGA is sensitive to on wake-up are programmable; that is, it is possible to ignore events on some PIOs but not others.

5 Microcontroller, memory, and baseband logic



enc1482336638614.2

Figure 5-1 Baseband digits block diagram

5.1 Microcontroller

The MCU, interrupt controller, and event timer run the Bluetooth software stack and control the Bluetooth radio and external interfaces. A 16-bit RISC microcontroller is used for low power consumption and efficient use of memory.

5.2 Memory

CSRB31024 LGA memory includes:

- RAM code and data (Internal)
- ROM (Internal)
- OTP (Internal)
- Flash (Internal)

Memory spaces include:

- Application Store: A storage area for customer applications, located in OTP or SPI flash.
- Configuration Store: An area of memory used to store configuration settings (ROM, OTP, RAM, SPI flash).
- User Store: OTP (programmable once then read-only) and SPI flash data storage available to user applications at runtime.

5.2.1 RAM code and data (Internal)

CSRB31024 LGA has RAM for code and data.

NOTE Either RAM is available for code or data.

Code RAM

- 64 KB: For code or data
- Primary use for developing applications for eventual storage in OTP memory
- Useable as a cache for applications stored in flash or OTP memory
- Useable as code or data RAM if not used as a code cache
- Software provides details of the area of shared RAM to the user application
- Part or all of the code RAM is powered down to save power when not in use

Data RAM

- 16 KB: For code or data
- Primary use for firmware and applications
- The use of all data RAM for executing code is possible (although there are some restrictions on when this can be done)

5.2.2 ROM (Internal)

System firmware is implemented in 192 KB of internal ROM.

NOTE Code executes from ROM and RAM.

5.2.3 OTP (Internal)

60 KB of OTP is available for storage of user applications:

- One-time programmable
- Enables reading and writing of information to the configuration store
- Enables downloading of software
- Has a storage provider driver
- PMU supplies power
- Useable space to store a boot loader or fall-back image for deploying updateable applications in Flash

5.2.4 Flash (Internal)

256 KB of flash (internal) memory is available for user applications:

- More than 100,000 erase/write cycles[1].
- Internal flash is accessed at a speed lower than the processor can run: This means that application code executing from flash executes slower than that in OTP (or RAM). To mitigate this use code RAM as a cache.

  NOTE For information about flash configuration, see *CSR102x Initial Configuration for Devices* (80-CF263-1) (part of Qualcomm Bluetooth Low Energy SDK).
- Encrypted applications have a maximum size of 64 KB. This is because the image is copied to the code RAM and decrypted in place using the decryption key stored in OTP. For more information, see the SDK software release note.
- Up to 20 years data retention[1].

[1] Erase/write cycle and data retention are trade-off parameters, and dependent on application mission profiles, for example temperature.

6 Peripheral interfaces

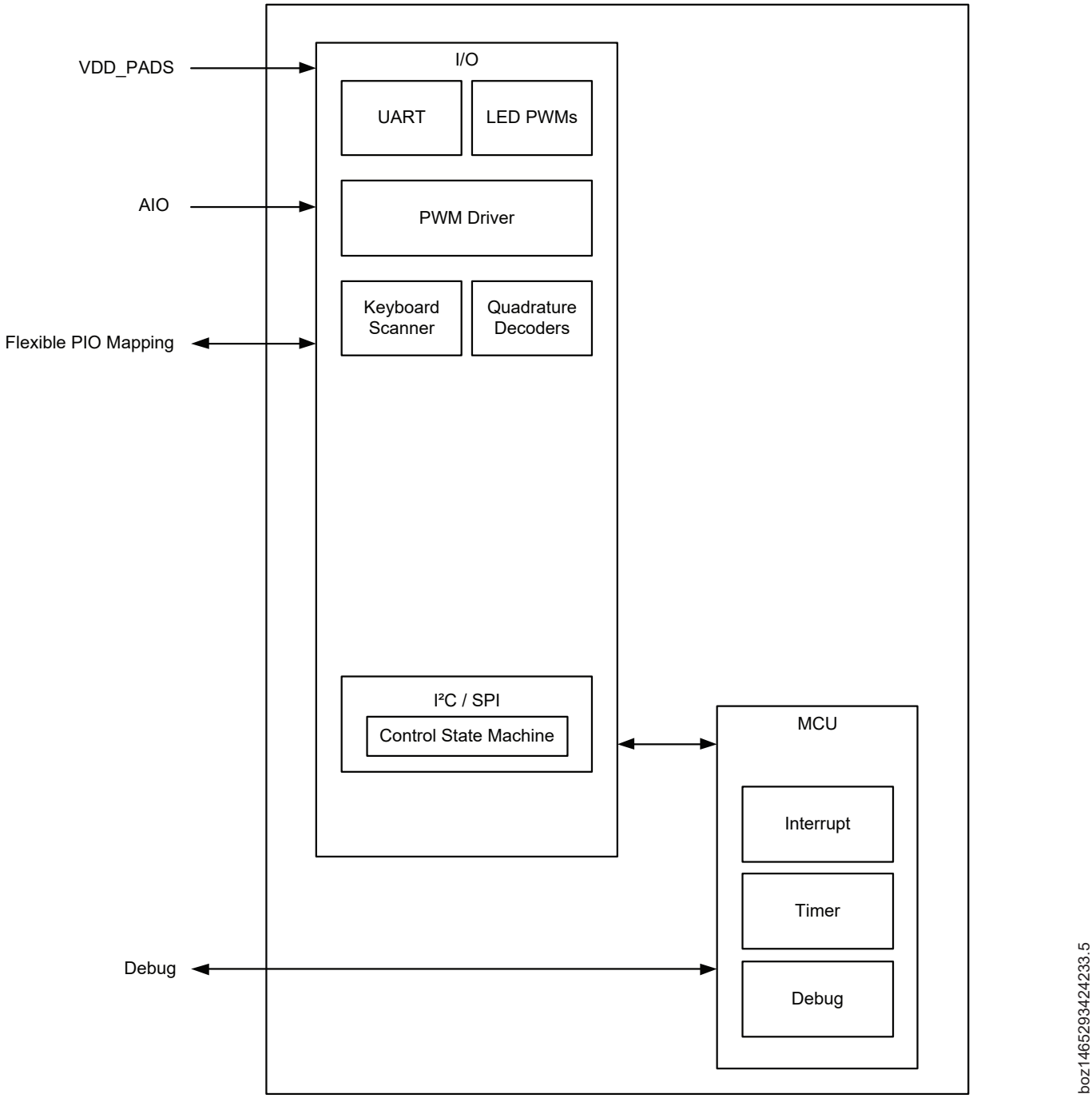


Figure 6-1 Peripheral interfaces block diagram

6.1 I²C Master/Slave (General)

CSRB31024 LGA has 1 I²C master/slave general interface for communication with external peripherals and sensors:

- Maximum clock speed 1 MHz
- Data transmiting/receiving of variable byte length
- 7-bit and 10-bit addressing modes
- Configurable:
  - PIO pins for SCL and SDA
  - I²C clock: 100 kHz default (software-configurable) at 1:1 duty-cycle (asymmetric if necessary)
  - Supports slave clock stretching
  - CSRB31024 LGA is Fast Mode and Fast Mode+ compatible.

NOTE Strong pull-up is typically sufficient for I²C on all PIO pads.

6.2 SPI Master/Slave (General)

CSRB31024 LGA has one SPI master/slave general interface for communication with other devices.

CSRB31024 LGA supports:

- SPI master and slave
- All four modes supported
- Two methods of transferring data to memory:
  - DMA to/from memory:
    - 8-bit or 16-bit word size
    - Big and little-endian
  - Software reads and writes to FIFOs: variable from 1-bit to 16-bits
- Interrupt callbacks to processor enable SPI as a slave to indicate that it requires service
- Deep sleep mode (depending on clock)

Figure 6-2 shows a simple SPI timing diagram.

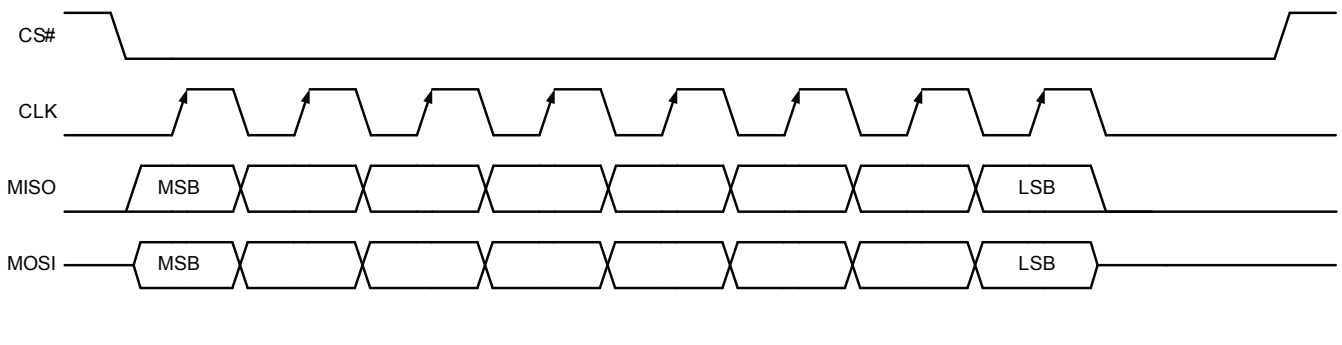


Figure 6-2 SPI timing diagram

6.3 SPI debug interface (QTIL proprietary)

NOTE The CSRB31024 LGA debug SPI interface is available in SPI slave mode to enable an external MCU to program and control the CSRB31024 LGA, via libraries or tools supplied by QTIL. The protocol of this interface is proprietary. A 128-bit lock key is applicable to secure the application code. The four SPI debug lines directly support this function on PIO[3:0].

Debug SPI access is required for programming, configuring and debugging the CSRB31024 LGA. It is required in production. Ensure the four SPI signals and SPI_PIO# are brought out to either test points or a header with SPI_PIO#.

To enable the SPI debug feature on PIO[3:0], take SPI_PIO# high.

CSRB31024 LGA uses a 16-bit data and 16-bit address programming and debug interface. Transactions occur when the internal processor is running or is stopped.

Data is written or read one word at a time, or the auto-increment feature is available for block access.

6.3.1 Instruction cycle

The CSRB31024 LGA is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 6-1 lists the instruction cycle for an SPI transaction.

Table 6-1 Instruction cycle for an SPI transaction

Number	Transaction	Instruction
1	Reset the SPI interface	Hold SPI_CS# high for 2 SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word/s
5	Termination	Take SPI_CS# high

Except for reset, hold SPI_CS# low during the transaction. Data on SPI_MOSI is clocked into the CSRB31024 LGA rising edge of the clock line SPI_CLK. When reading, CSRB31024 LGA replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

The auto increment operation on the CSRB31024 LGA cuts down on the overhead of sending a command word and the address of a register for each read or write. This is especially true when large amounts of data are to be transferred. The auto increment offers increased data transfer efficiency on the CSRB31024 LGA. To invoke auto increment, SPI_CS# is kept low, which auto increments the address while providing an extra 16 clock cycles for each extra word written or read.

6.3.2 Multislave operation

Do not connect the CSRB31024 LGA in a multislave arrangement by simple parallel connection of slave MISO lines. When CSRB31024 LGA is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, CSRB31024 LGA may output 0 if the processor is running or 1 if it is stopped.

6.4 UART (General)

The CSRB31024 LGA UART interface provides a simple mechanism to communicate with other serial devices using the RS232 protocol.

Table 6-2 lists the four signals that implement the UART function in CSRB31024 LGA. Hardware flow control using RTS/CTS lines is optional.

Table 6-2 UART signals

Signal	Description
UART_RX	Pin to receive UART data from another device
UART_TX	Pin to transmit UART data to another device
UART_CTS	Pin for another device to indicate it is ready to receive data (active low input)
UART_RTS	Pin for another device to indicate that this other device is ready to receive data (active low input)

6.4.1 UART configuration settings

UART configuration parameters, for example baud rate and data format, are set using CSRB31024 LGA firmware.

Table 6-3 lists UART configuration settings for CSRB31024 LGA.

Table 6-3 UART configuration settings

Parameter		Possible values	
Baud rate[a]	Internal RC clock	≤ 7200	<2 % Error
		7200 < baud ≤ 115200	<5 % Error
	XTAL clock	> 115200	<1 % Error
Parity		None, Odd or Even	
Number of stop bits		1 or 2	
Bits per byte		8	

[a] For more information, see the SDK release note.

6.4.2 UART configuration while in Deep Sleep

The maximum baud rate is 2400 baud during deep sleep.

6.5 PWMs

CSRB31024 LGA has five independently configurable PWM instances.

A multipurpose PWM generator provides two modes:

- Normal PWM mode:
  - For motor control and general-purpose PWM
- LED mode:
  - For LED fading

6.5.1 LED control PWM

CSRB31024 LGA has four LED mode PWM blocks (2 x fast / 2 x slow). Each LED mode PWM has an 8-bit resolution for all configuration registers and a:

- Minimum brightness duty cycle (grouped in a 16-bit wide register)
- Maximum brightness duty cycle (grouped in a 6-bit wide register)

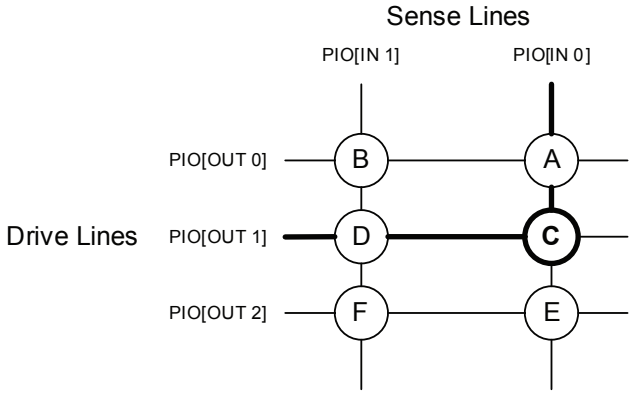
- Hold Minimum and Maximum time (grouped in a 16-bit wide register)
- Step (ramp) time
- Brightness configuration specified in units of typically 30 µs assuming a 32 kHz clock
- Hold times specified in units of typically 16 ms assuming a 32 kHz clock
- Step time specified in units of typically 1 ms assuming a 32 kHz clock

NOTE CSRB31024 LGA supports immediate reconfiguration on the sync register write.

6.6 Key scanner

CSRB31024 LGA has one key scanner for applications such as mouse and keyboard HID.

Figure 6-3 shows an example keyboard matrix at a size of 3 x 2 (PIO drive lines x PIO sense lines respectively).



tuv1480083208101.2

Figure 6-3 Example keyboard matrix 3 x 2 size

Physical buttons are on line crossings A to F. If a button is pressed both lines become connected. Assuming sense lines are pulled-up by internal logic, a keypress, for example C is detectable by forcing PIO[OUT 1] low and reading 0 on PIO[IN 0].

It supports:

- Keypad matrix up to 12 PIO inputs (sense lines) and 18 PIO outputs (drive lines):
  - Drives 1 to 18 drive lines consecutively
  - 12-bit key registers updated every scan
- Press and release events reported to the host via callback
- Variable scan rate:
  - By default drives consecutive drive lines every clock cycle
  - Configurable number of clocks per drive line

NOTE The key scanner does not support ghost key removal.

The key scanner configuration and control includes:

- PIO pin numbers to be used for drive and sense lines
- Scan rate, Hz, and active/idle ratio
- Hardware starting and stopping
- Callback creation to receive keyboard map data.

6.7 Quadrature decoders

CSRB31024 LGA has four quadrature decoders with:

- Each having a configurable simple filter on inputs (for debouncing)
- Enabling and disabling of single or multiple decoders
- Data reading functionality
- Processor interrupt generation

6.8 10-bit auxiliary ADC

CSRB31024 LGA has a single 10-bit auxiliary ADC:

- A resistive SAR ADC
- Attached to one AIO pad
- The processor has access to its ADC result value after exit from Deep Sleep mode
- The ADC reference is VDD_AUX, see Figure 6-4.

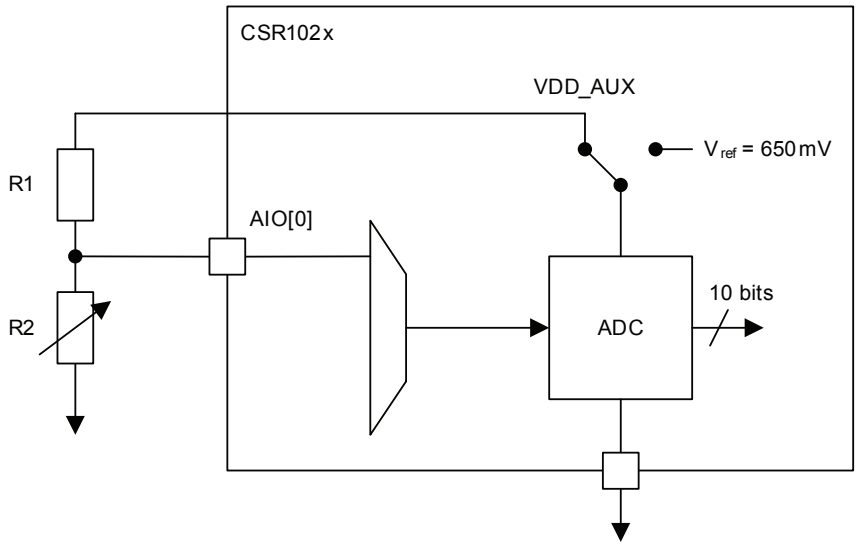


Figure 6-4 10-bit auxiliary ADC reference

NOTE Figure 6-4 shows an extra internal 650 mV reference. This is for QTIL test purposes only.

The 10-bit Auxiliary ADC is not available during XTAL start up or battery voltage and temperature monitoring. Therefore, if the hardware is already using the ADC, the time to perform a conversion may be longer.

7 Auxiliary features

7.1 Battery monitor

CSRB31024 LGA contains an internal battery monitor that reports the battery voltage to the software.

7.2 Temperature sensor

CSRB31024 LGA contains a sensor that can report the chip temperature in °C using a firmware API.

8 Programmable I/O ports, PIO, and AIO

This section describes CSRB31024 LGA PIO and AIO.

8.1 General PIOs

15 lines of programmable bidirectional I/O are provided:

- May be set by the application code or used as an input or to wake the chip.
- Software-configurable as weak pull-up, weak pull-down, strong pull-up, or strong pull-down.
- At reset all lines are inputs with weak pull-down.
- Pull strength, direction, and pad states preserved across all nonoff states to support waking on any PIO (even when VDD_DIG is powered down).
- Configurable to wake CSRB31024 LGA via an individually selectable mask for rising, falling or any edge transition from Deep Sleep: No RAM Retention and External Interrupts Enabled, Deep Sleep: 16 KB Data RAM Retention or Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention mode.
- Available as interrupt request lines.
- Powered from VDD_PADS

NOTE VDD_PADS must remain powered.

QTIL cannot guarantee that the PIO assignments remain as described. Implementation of the PIO lines is firmware build-specific, for more information see the relevant software release note.

8.2 AIOs

CSRB31024 LGA has one pin providing a unidirectional analog programmable input line, AIO[0].

NOTE This pin does not provide an output capability.

8.2.1 10-bit auxiliary ADC

Table 8-1 CSRB31024 LGA 10-bit auxiliary ADC

10-bit auxiliary ADC	Min	Typ	Max	Unit
Resolution	-	-	10	Bits
Input voltage range[a]	0	-	VDD_AUX	V
Input bandwidth	-	100	-	kHz
Conversion time	1.38	1.69	4.14	µs
Sample rate[b]	-	-	700	Samples/s

[a] LSB size = VDD_AUX/1023.
[b] The 10-bit auxiliary ADC is accessed through the firmware API. The sample rate given is achieved as part of this function.

8.3 Digital pin states on initial power-up

Table 8-2 shows the pin states of CSRB31024 LGA on initial power-up. Pull-up and pull-down default to weak values unless specified otherwise.

Table 8-2 Pin states on initial power-up

Pin name / Group	On initial power-up
SPI_PIO#	Strong Pull-Down
All other PIOs	Weak Pull-Down

8.4 PIO configuration options

Table 8-3 lists CSRB31024 LGA PIO configuration options.

Table 8-3 CSRB31024 LGA PIO configuration options

PIO pin	I²C master only	SPI (General)				Debug SPI	UART (General)		Quadrature decoder input[a]		LED/PWM[b]	KeyScan		TMRCTR	
		CLK	CS#	MISO	MOSI		Data	Flow	A	B		Drive	Sense	Timer 0	Timer 1
PIO[14]	SCL	Y	Y	Y	Y	-	TX	RTS	Y	Y	Y	Y	Y	Y	Y
PIO[13]	SDA	Y	Y	Y	Y	-	RX	CTS	Y	Y	Y	Y	Y	Y	Y
PIO[12]	SCL	Y	Y	Y	Y	-	TX	RTS	Y	Y	Y	Y	Y	Y	Y
PIO[11]	SDA	Y	Y	Y	Y	-	RX	CTS	Y	Y	Y	Y	Y	Y	Y
PIO[10]	SCL	Y	Y	Y	Y	-	TX	RTS	Y	Y	Y	Y	Y	Y	Y
PIO[9]	SDA	Y	Y	Y	Y	-	RX	CTS	Y	Y	Y	Y	Y	Y	Y
PIO[8]	SCL	Y	Y	Y	Y	-	TX	RTS	Y	Y	Y	Y	Y	Y	Y
PIO[7]	SDA	Y	Y	Y	Y	-	RX	CTS	Y	Y	Y	Y	Y	Y	Y
PIO[6]	SCL	Y	Y	Y	Y	-	TX	RTS	Y	Y	Y	Y	Y	Y	Y
PIO[5]	SDA	Y	Y	Y	Y	-	RX	CTS	Y	Y	Y	Y	Y	Y	Y
PIO[4]	SCL	Y	Y	Y	Y	-	TX	RTS	Y	Y	Y	Y	Y	Y	Y
PIO[3]	SDA	Y	Y	Y	Y	MISO	RX	CTS	Y	Y	Y	Y	Y	Y	Y
PIO[2]	SCL	Y	Y	Y	Y	MOSI	TX	RTS	Y	Y	Y	Y	Y	Y	Y
PIO[1]	SDA	Y	Y	Y	Y	CS#	RX	CTS	Y	Y	Y	Y	Y	Y	Y
PIO[0]	SCL	Y	Y	Y	Y	CLK	TX	RTS	Y	Y	Y	Y	Y	Y	Y

[a] Quadrature decoder input A and B both require 4 PIOs to be assigned.
[b] LED/PWM require 5 PIOs to be assigned to access all functionality.

9 CSRB31024 LGA software stack

CSRB31024 LGA is supplied with Bluetooth v5.0 specification compliant stack firmware. Figure 9-1 shows that the CSRB31024 LGA software architecture enables the Bluetooth processing and the application program to run on the internal RISC MCU.

NOTE CSRB31024 LGA is supported in the SDK from Version 3.1.2.

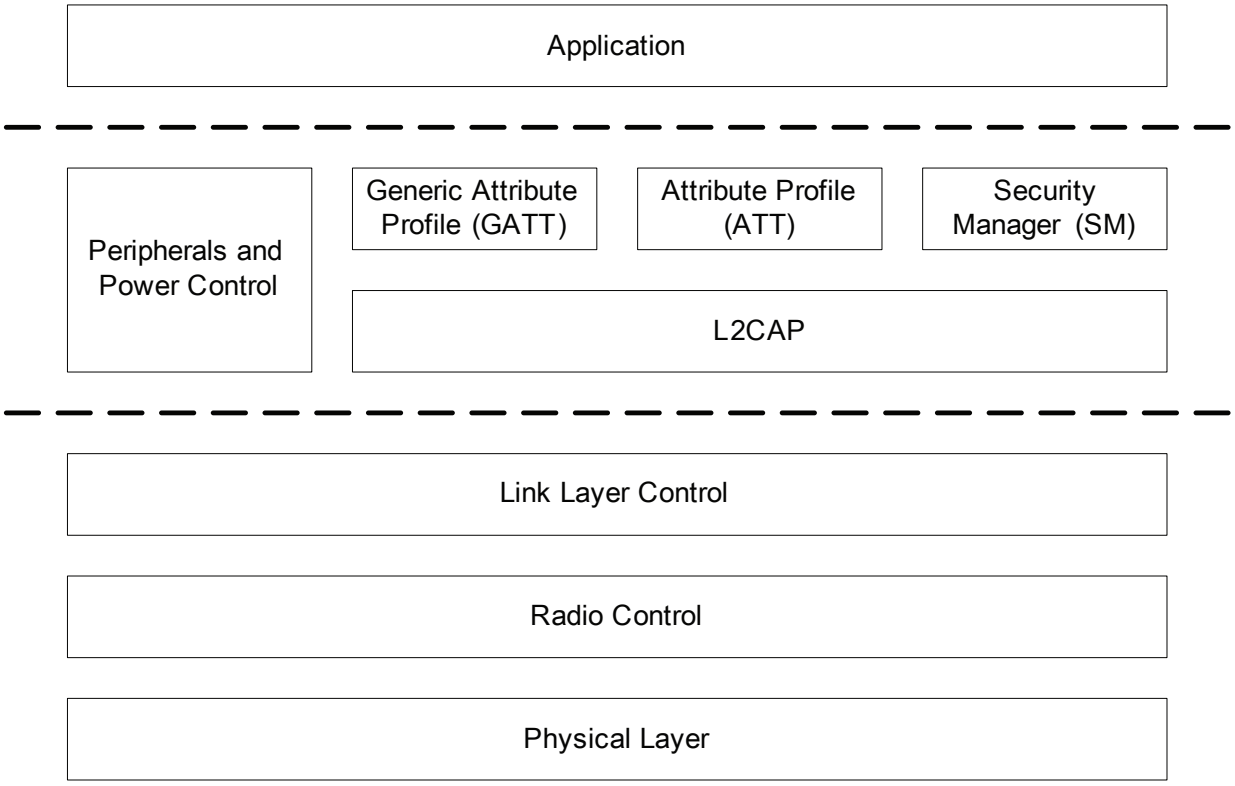


Figure 9-1 Software architecture

10 Power control and regulation

CSRB31024 LGA contains a switch-mode regulator that generates all the supply rails required from the battery.

10.1 Switch-mode regulator

The switch-mode regulator generates the four output voltage rails from the battery supply, VDD_BAT.

The switch-mode regulator generates all required voltage rails for the system to operate using only a single inductor. No user intervention is required; the regulator automatically changes from buck to boost mode depending on the battery voltage and output voltage of the rails.

The voltage output is dynamically changed dependent on the mode of operation.

NOTE Each rail is only charged when, after sampling, it is below the comparator threshold.

10.2 Reset

CSRB31024 LGA processor is reset by:

- Power-on reset
- Software-configured watchdog timer
- Exit from Deep Sleep: No RAM Retention and External Interrupts and Timer Enabled (Hibernate) mode
- Exit from Deep Sleep: No RAM Retention and External Interrupts Enabled (Dormant) mode

The PMU is reset by exit from Deep Sleep: No RAM Retention and External Interrupts Enabled (Dormant) mode.

To fully reset the PIO pads take all of VDD_PADS, VDD_BAT, VDD_AUX, VDD_RAD and VDD_MEM pins below 0.4 V.

If VDD_BAT is removed from CSRB31024 LGA while not in Deep Sleep: No RAM Retention and External Interrupts Enabled (Dormant) mode, the PIO pads must be fully reset as described.

NOTE VDD_BAT input voltage must drop to 0.4 V to guarantee a rising VDD_BAT is seen by the PMU on re-assertion.

VDD_BAT typically takes approximately 20 s to drop to 0 V when power is removed due to circuit decoupling capacitance.

11 CSRB31024 LGA example application schematic

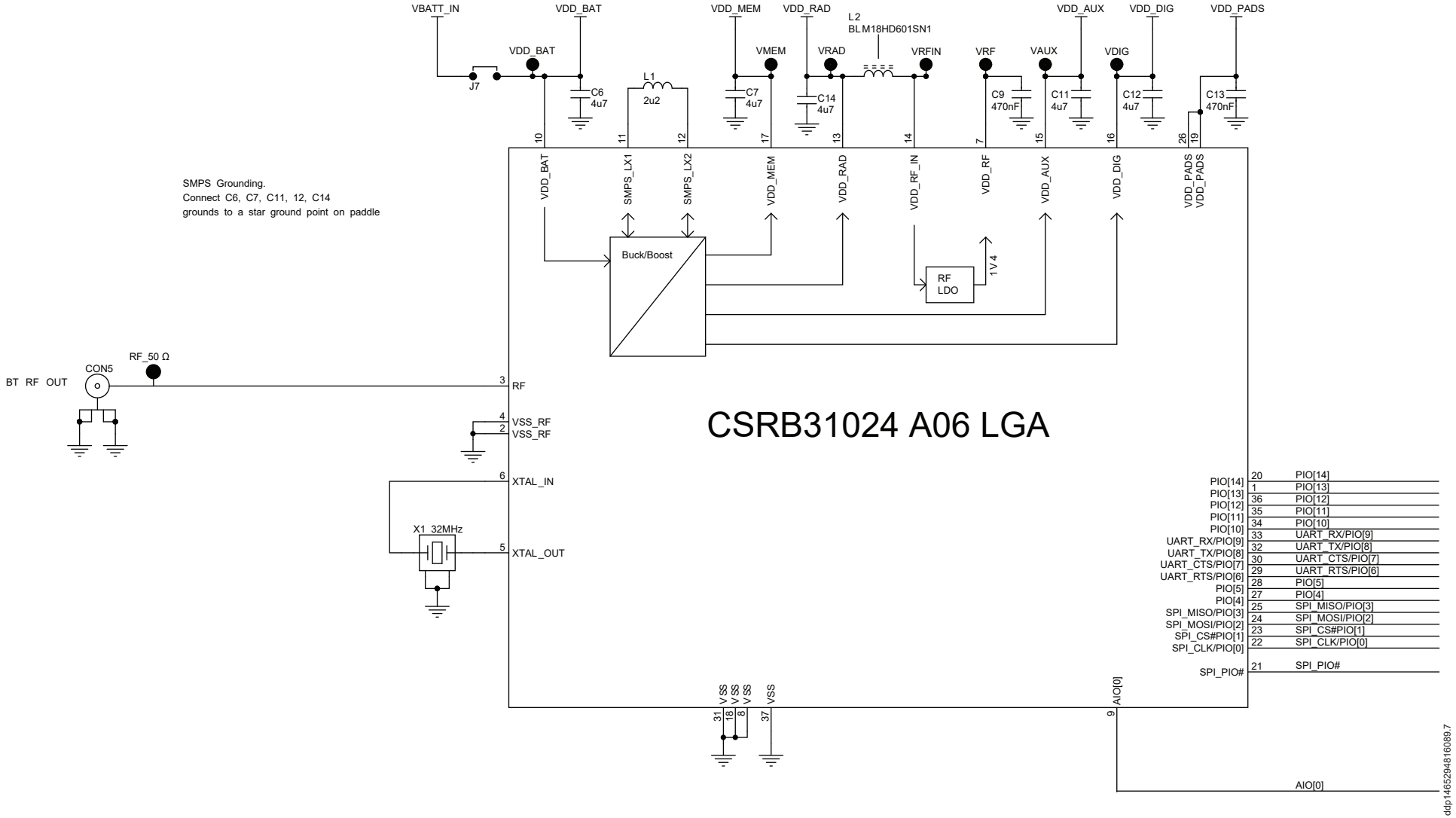


Figure 11-1 CSRB31024 LGA example application schematic

12 Electrical characteristics

12.1 Absolute maximum ratings

NOTE Exceeding absolute maximum ratings causes permanent damage to the CSRB31024 LGA. Exposure to any absolute maximum rating for extended periods of time affects reliability.

Table 12-1 CSRB31024 LGA absolute maximum ratings

Rating	Min	Typ	Max	Unit
Storage temperature	-40	-	85	°C
Battery (VDD_BAT and VDD_PADS)	0	-	3.6	V
I/O supply voltage	0	-	3.6	V
I/O supply (VDD_PADS) total current	-	-	30	mA
VDD_AUX, VDD_DIG, AIOs	0	-	1.26	V
VDD_RAD, VDD_RF_IN, VDD_RF	0	-	2.2	V
XTAL_IN, XTAL_OUT	0	-	0.8	V
RF	-	-	0	dBm

12.2 Recommended operating conditions

Use the CSRB31024 LGA recommended operating conditions to ensure optimum performance and reliability.

Table 12-2 CSRB31024 LGA recommended operating conditions

Operating condition	Min	Typ	Max	Unit
Operating temperature range	-40	20	85	°C
Battery (VDD_BAT)	2.7	3.0	3.3	V
I/O supply voltage (VDD_PADS)	2.7	3.0	3.3	V
RF (maximum input level)	-10	-5	-	dBm

12.3 Input/output terminal characteristics

Always comply with the stated values when attaching external components to the CSRB31024 LGA.

NOTE Current drawn by a pin is positive (+), current supplied is negative (-).

12.3.1 Switch-mode regulator

CSRB31024 LGA power supply rails are generated from a single pin connection to the battery, VDD_BAT. Minimum decoupling should be 4.7 µF using the same low ESR components as the output capacitors.

For supplies that have high resistance (greater than 30 Ω), such as CR2032 coin cells, large value decoupling may be used. When powered from high impedance sources, while CSRB31024 LGA changes operational modes, 22 µF can significantly reduce voltage variation on VDD_BAT.

The outputs of the Switch-mode Regulator require adequate decoupling. 4.7 µF components are recommended, in order that a real capacitance of 3 µF is presented to the chip based on a DC bias voltage derating of 3 V_{DC} with AC200 mVrms.

NOTE Specifically 0402 components are not acceptable; PCB layout should use 0603 footprints. The component BOM should call for capacitors with a body thickness >0.65 mm.

Both the capacitance and ESR lead to observed output ripple:

- A suitable ESR at 1 MHz should be under 0.10 Ω.

All power is delivered through the 2.2 µH power inductor. To achieve good stability and efficiency use:

- Saturation current (I_{sat}) of more than 800 mA
- DC resistance (DCR) of less than 0.25 Ω.

NOTE Switching frequency is variable based on the load of each rail.

PCB assembly rework is not permitted on switch-mode output capacitors or inductor. An open circuit on these components even for a short time may result in damage to CSRB31024 LGA.

Table 12-3 CSRB31024 LGA switch-mode regulator

Switch-mode regulator	Min	Typ	Max	Unit
Output voltage (VDD_AUX)[a]	-	1.2	-	V
Output voltage (VDD_DIG)[a]	-	1.1	-	V
Output voltage (VDD_RAD)[a]	-	1.8	-	V
Output voltage (VDD_MEM)[a]	-	3.3	-	V

[a] These are internal regulators and should have no additional load or source connected.

12.3.2 RF linear regulator

Table 12-4 CSRB31024 LGA RF linear regulator

Normal operation	Min	Typ	Max	Unit
Input voltage (VDD_RF_IN)	1.2	-	2.2	V
Output voltage (VDD_RF)	1.0	-	2.0	V

NOTE This regulator is for QTIL internal use only of the RF rail.

It is necessary to fit a ferrite between the output of the switch mode (VDD_RAD) and the input of the linear regulator (VDD_RF_IN). QTIL recommends BLM18HD601SN1.

12.3.3 Digital I/O terminals

Table 12-5 CSRB31024 LGA input voltage levels

Input voltage levels	Min	Typ	Max	Unit
V_{IL} input logic level low	-	-	25% x VDD_PADS	V
V_{IH} input logic level high	75% x VDD_PADS	-	-	V

Table 12-6 CSRB31024 LGA output voltage levels

Output voltage levels	Min	Typ	Max	Unit
V_{OL} output logic level low, I_{OL} = 8.0 mA (Max Drive Strength)	-	-	20% x VDD_PADS	V
V_{OH} output logic level high, I_{OL} = -8.0 mA (Max Drive Strength)	80% x VDD_PADS	-	-	V
T_r/T_f (for 30 pF load)	-	-	2	ns

Table 12-7 CSRB31024 LGA input and tri-state

Input and tri-state	Min	Typ	Max	Unit
With strong pull-up	3.5	4.7	6.0	kΩ
With strong pull-down	3.5	4.7	6.0	kΩ
With weak pull-up[a]	8	40	50	µA
With weak pull-down[a]	10	40	50	µA
C_I input capacitance	-	5	-	pF

[a] Range applicable for VDD_PADS between 1.8 V and 3.3 V when measured as a short circuit.

12.3.4 AIO

Table 12-8 CSRB31024 LGA AIO

Input/output voltage levels	Min	Typ	Max	Unit
Input voltage	0	-	VDD_AUX	V

13 Current consumption

Table 13-1 shows CSRB31024 LGA total typical current consumption measured at the battery.

Table 13-1 Current consumption

Mode	Description	Total typical current at 3 V[a]
Deep Sleep: No RAM Retention and External Interrupts Enabled (Dormant)	All functions are shut down. To wake the chip, toggle a preconfigured PIO.	1.6 µA
Deep Sleep: No RAM Retention with External Interrupts and Timer Enabled (Hibernate)	VDD_PADS = ON VDD_BAT = ON	5.5 µA
Deep Sleep: 16 KB Data RAM Retention	VDD_PADS = ON VDD_BAT = ON RAM = ON Digital Circuits = ON SMPS = ON	10.5 µA
Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention	VDD_PADS = ON VDD_BAT = ON RAM = ON Digital Circuits = ON SMPS = ON	12 µA
Idle: Shallow Sleep	VDD_PADS = ON VDD_BAT = ON RAM = ON Digital Circuits = ON MCU = IDLE <1 µs Wake-up Time	0.75 mA
Idle: Active	VDD_PADS = ON VDD_BAT = ON RAM = ON Digital Circuits = ON	1.3 mA (Execution from Cache) 13.5 mA (Active SMEM Execution)
Tx Active	0 dBm Transmit Power	5 mA Average
Rx Active	-90.0 dBm Sensitivity	5 mA Average

[a] These are indicative values only. For accurate values see the appropriate software release note for this device.

14 Product reliability tests

The reliability tests in this section follow the tests outlined in AEC-Q100 and shall be performed on CSRB31024 LGA in QFN 32-lead 5 x 5 x 0.6 mm, 0.5 mm pitch I/O. QTIL may use data from structurally similar products to meet some requirements. Where this is done, the usage shall be recorded in the device reliability test report.

This package qualification will (where moisture sensitivity preconditioning is required) use JEDEC J-STD-020, JESD22- A113, MSL3.

14.1 Automotive die test

Table 14-1 Automotive die test

Test	Test conditions	Specification
ESD, Human Body Model	Class 1C - RF lead, Class 1B - All other leads	AEC Q100-002
ESD, Charged Device Model	Class C4B	AEC Q100-011 / JEDEC JS-001-2017
Latch-up	±100 mA, 1.5 x VDD_{max}, ambient and max operation temperature	AEC Q100-004D
Early Life Failure Rate	T_a = 110°C, VDD_{max}, 48 hours	AEC Q100-008
High Temperature Operating Life	T_a = 110°C, VDD_{max}, 1000 hours	JEDEC JESD22-A108

14.2 Automotive package test

Table 14-2 Automotive package test

Test	Test conditions	Specification
Moisture Sensitivity Preconditioning	30°C / 60% RH, 192 hours	JEDEC J-STD-020, JESD22-A113
Temperature Cycling	-65ºC to 150ºC, 500 cycles, 1000 cycles	JEDEC JESD22-A104
Biased Highly Accelerated Stress Test (HAST)	110ºC / 85% RH, VDD_{max}, 264 hours, 528 hours	JEDEC JESD22-A110
High Temperature Storage Life	150ºC, 1000 hours, 2000 hours	JEDEC JESD22-A103

14.3 Life testing production limitations

NOTE For more information about CSRB31024 LGA qualification, see the *CSRB31024 LGA Automotive Qualification Report* (80-CG639-1).

14.3.1 Early life fail rate

Table 14-3 lists the activity voltage profile used for the CSRB31024 LGA test application.

Table 14-3 Test application activity voltage profile for early life fail rate

Mode	On: Active	On: Deep Sleep	Off
Activity (%)	0.80 * 92% = 73.6	0.20 * 92% = 18.4	8.0
Digital Voltage (V)	1.1	0.85	0.0

Environmental conditions:

- Test Temperature = 110°C
- Test Voltage = Typical
- Test Duration = 48 Hours
- Unit count = 2400

14.3.2 High temperature life testing

Table 14-4 lists the activity voltage profile used for the CSRB31024 LGA test application.

Table 14-4 Test application activity voltage profile for high temperature life testing

Mode	On: Active	On: Deep Sleep	Off
Activity (%)	0.80 * 92% = 73.6	0.20 * 92% = 18.4	8.0
Digital Voltage (V)	1.1	0.85	0.0

Environmental conditions:

- Test Temperature = 110°C
- Test Voltage = Typical
- Test Duration = 1000 Hours
- Unit count = 240

14.3.3 HTOL: Mission profile analysis (Grade 3)

Expected product life can be calculated by considering the duration in each mode integrated over the operational temperature:

- Life = 8000 hours within 15 year duration

Table 14-5 lists an example temperature profile. When this is applied to CSRB31024 LGA using an Arrhenius equation, a maximum On: Active duty cycle of 100% is achieved for life.

CAUTION Applications that require a more aggressive life-time temperature profile should scale back the On: Active duration.

Calculate your total On: Active life expectancy for CSRB31024 LGA using your product usage expectations. It is not recommended to use CSRB31024 LGA beyond the parameters described in this section. If your use case extends beyond these parameters, contact your local Qualcomm® Account Manager with a clear description of your use case and request feedback from Qualcomm Quality and Product Management before you proceed with your design.

Table 14-5 Example life-time temperature profile

Ambient Temperature / °C	Distribution / %
-40	6.0
23	20.0
50	65.0
85	9.0

15 Environmental declaration statement for QTIL semiconductor products

This declaration statement applies to QTIL products.

QTIL semiconductor products and packing materials meet the following substance restriction requirements, including Table 15-1:

- EU RoHS Directive 2011/65/EU[2] maximum concentration values
- EU REACH, Regulation (EC) No 1907/2006[2]:
  - List of substances subject to authorization (Annex XIV)
  - Restrictions on the manufacture, placing on the market and use of certain dangerous substances, preparations, and articles (Annex XVII)
- POP regulation (EC) No 850/2004[2]
- EU Packaging and Packaging Waste, Directive 94/62/EC[2]
- Montreal Protocol on substances that deplete the ozone layer
- “California Prop 65”

Table 15-1 Restricted substances present in QTIL products

Found in products	Substances	CAS no.	Amount present, ppm	Applicable regulations
WLP packaged	N-Methyl pyrrolidone	872-50-4	150-210	REACH SVHC, Prop 65

QTIL products contain less than 900 ppm of bromine or chlorine and less than 1500 ppm of bromine and chlorine combined in each homogeneous material (BrCl-free).

For more information about QTIL responsible product design, including substances QTIL avoids, refer to the *Product Responsibility* section of the Qualcomm® website: http://www.qualcomm.com.

[2] Applicable amendments as published in the EU Official Journal.

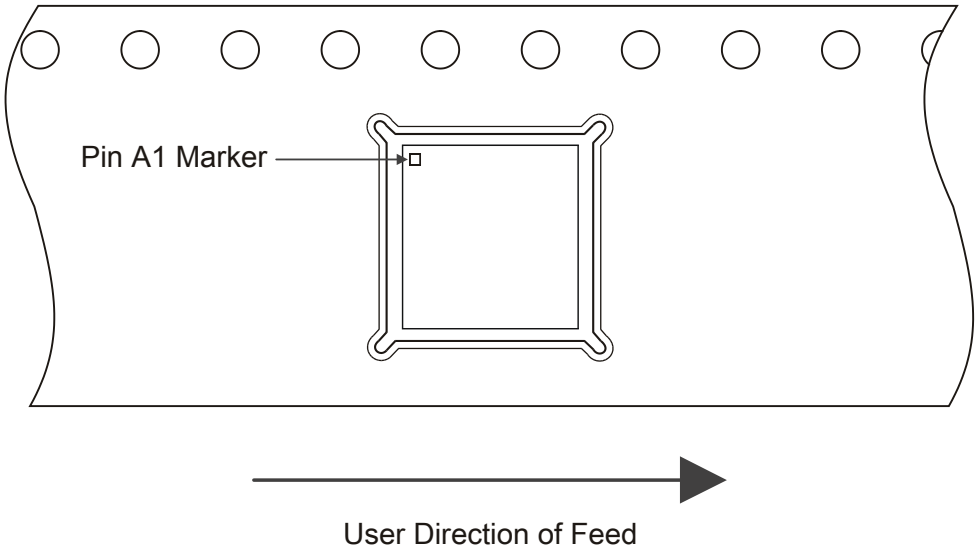
16 Tape and reel information

CSRB31024 LGA ICs are supplied on tape and reels.

For tape and reel packing and labeling, see *IC Packing and Labeling Specification* (80-CF403-1).

16.1 Tape orientation

Figure 16-1 shows the CSRB31024 LGA packing tape orientation.



eem14800832079612

Figure 16-1 CSRB31024 LGA tape orientation

16.2 Tape dimensions

Figure 16-2 shows and Table 16-1 lists the dimensions of the tape for the CSRB31024 LGA.

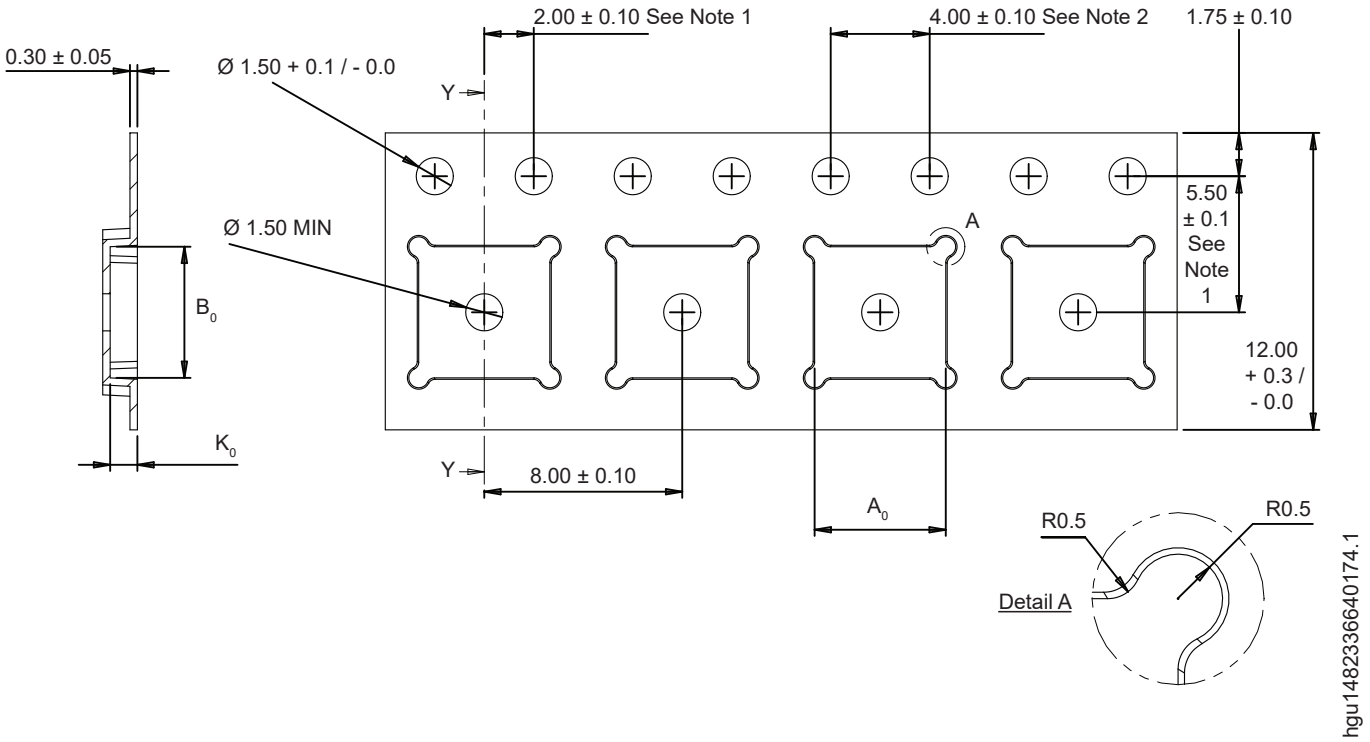


Figure 16-2 CSRB31024 LGA tape dimensions

Table 16-1 CSRB31024 LGA tape dimensions

A0	B0	K0	Unit	Notes
5.3 ± 0.1	5.3 ± 0.1	1.1 ± 0.1	mm	1. Measured from centerline of sprocket hole to centerline of pocket. 2. 10 sprocket hole pitch cumulative tolerance ±0.2.

16.3 Reel information

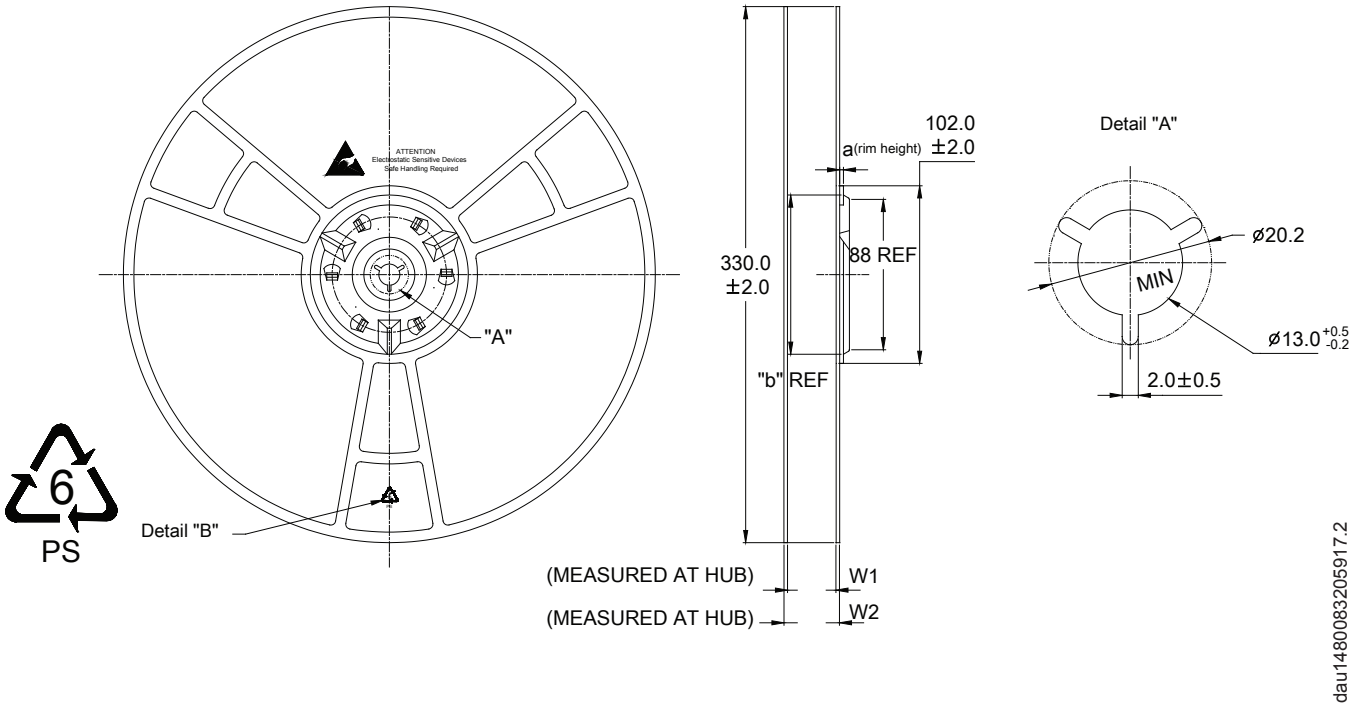


Figure 16-3 CSRB31024 LGA reel dimensions

Table 16-2 CSRB31024 LGA reel dimensions

Package type	Nominal hub width (Tape width)	a	b	W1	W2 max	Units
5 x 5 x 0.75 mm LGA	12	4.5	98.0	12.4 (2.0/-0.0)	18.4	mm

16.4 Moisture sensitivity level

CSRB31024 LGA is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

17 Document references

Document	Reference, date
Core Specification of the Bluetooth System	Bluetooth Specification Version 5.0, 06 December 2016
CSR102x Antenna Matching Application Note	80-CF404-1
CSR102x Initial Configuration for Devices	80-CF263-1
CSR102x / CSRB31024 Recommended Crystals Specification	80-CT924-1
CSRB31024 LGA Automotive Qualification Report	80-CG639-1
Charged Device Model (CDM) Electrostatic Discharge Test	AEC-Q100-011 Rev-C1, March 2013
Human Body Model Electrostatic Discharge Test	AEC-Q100-002 Rev-E, August 2013
IC Packing and Labeling Specification	80-CF403-1
Joint JEDEC/ESDA Standard for Electrostatic Discharge Sensitivity Test - Human Body Model (HBM) - Component Level	JS-001-2017, May 2017
Moisture / Reflow Sensitivity Classification for Nonhermitic Solid State Surface Mount Devices	IPC / JEDEC J-STD-020
Typical Solder Reflow Profile for Lead-free Devices Application Note	80-CT462-1

18 Terms and definitions

Term	Definition
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
AIO	Analog Input/Output
ATT	ATTribute protocol
B	Byte
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
Qualcomm® BlueCore™	Group term for QTIL's range of Bluetooth wireless technology ICs
BOM	Bill Of Materials
CSR™	Cambridge Silicon Radio
dBm	Decibels relative to 1 mW
EIA	Electronic Industries Alliance
ESD	Electrostatic Discharge
GAP	Generic Access Profile
GATT	Generic ATTribute protocol
GSM	Global System for Mobile communications
HID	Human Interface Device
I²C	Inter-Integrated Circuit Interface
I/O	Input/Output
IC	Integrated Circuit
IF	Intermediate Frequency
IPC	See www.ipc.org
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
KB	Kilobyte
L2CAP	Logical Link Control and Adaptation Protocol
LDO	Low (voltage) Drop-Out
LED	Light-Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
MAC	Medium Access Control
MCU	MicroController Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
NC	Not Connected or No Connection
NSMD	Non-Solder Mask Defined

Term	Definition
NVM	Non-Volatile Memory
OTP	One-Time Programmable
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PIO	Programmable Input/Output, also known as general purpose I/O
PMU	Power Management Unit
ppm	parts per million
PWM	Pulse Width Modulation
QTIL	Qualcomm Technologies International, Ltd.
RAM	Random Access Memory
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RX	Receive or Receiver
SDK	Software Development Kit
SMPS	Switch-Mode Power Supply
SPI	Serial Peripheral Interface
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage Controlled Oscillator