Qualcomm Technologies, Inc.

PMM8650AU/PMM8620AU

Data Sheet (for IoT)

80-82720-1 Rev. AC

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Device description

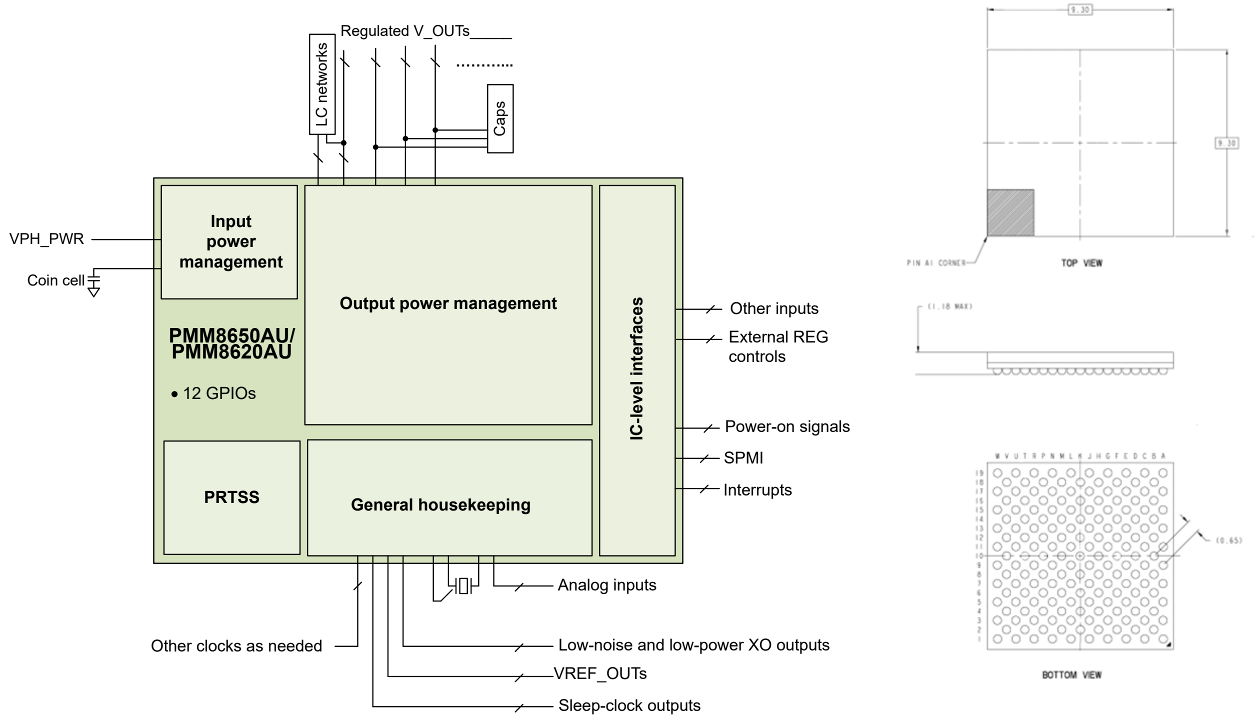
The PMM8650AU/PMM8620AU device integrates all the IoT product's power management, general housekeeping, and IC-level interface support functions into a single mixed-signal IC.

- System-clock and sleep-clock sources for the entire chipset
  - Three baseband (low-noise) output
  - Sleep clock output
- SPMI-M interface supporting both
  - Secondary communication with SoC
  - Primary communication with secondary PMICs
- Dedicated real-time subsystem
  - Real-time monitoring
  - Fault detection and fault aggregator
  - Data storage and event logging

Key features

- Nine fast transient SMPS
- Nine LDO linear regulators
- On-chip ADC
- Overtemperature protection
- 38.4 MHz XO controller and XO outputs
- Sleep clock and RTC with alarm
- SPMI-M
- 12 GPIOs
- I^2C
- MSP181

PMM8650AU/PMM8620AU high-level block diagram and 181 MSP outline drawing



Contents

Tables

Figures

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

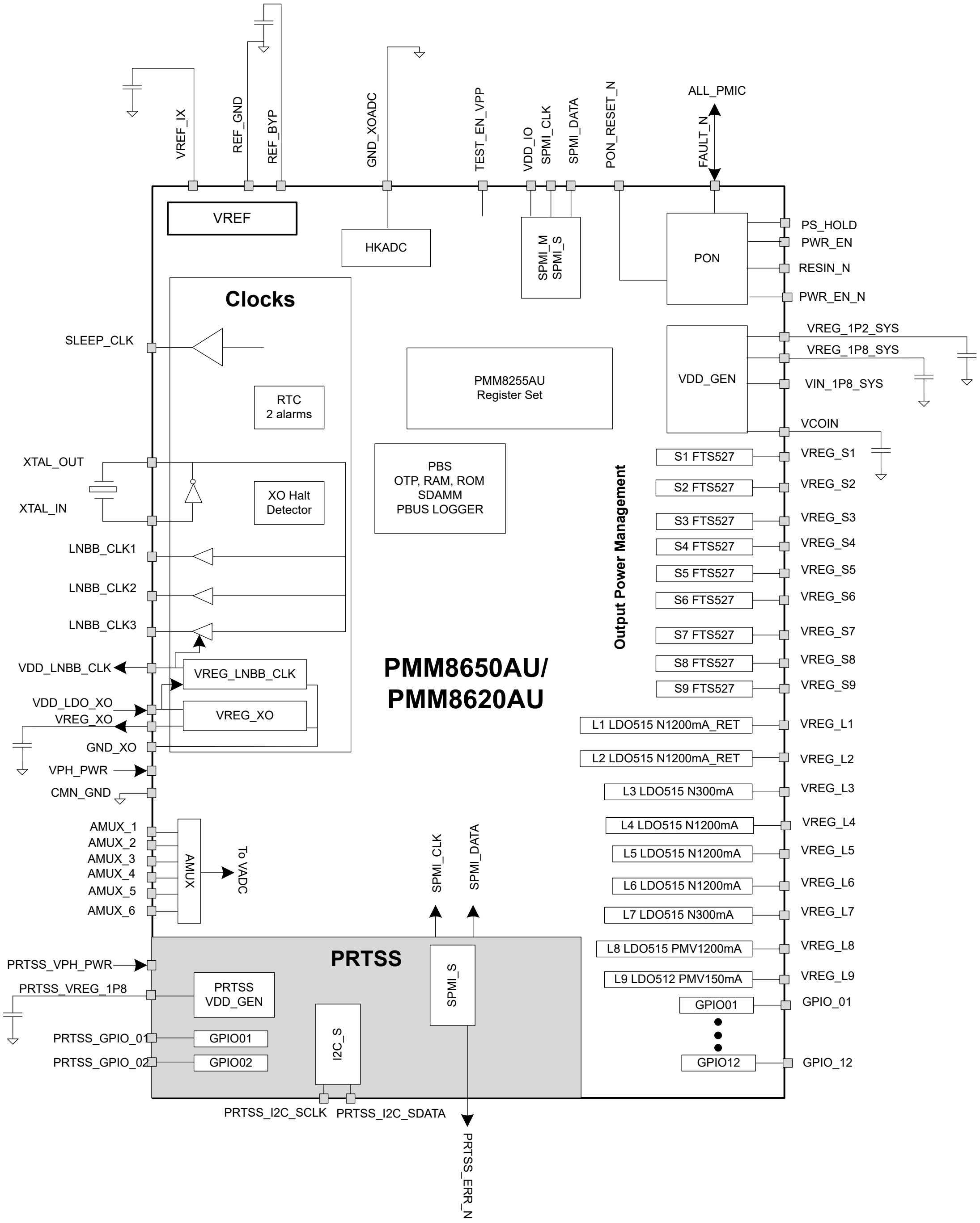


Figure 1-1 PMM8650AU/PMM8620AU functional block diagram and example application

1.2 PMM8650AU/PMM8620AU features

NOTE Some of the hardware features integrated within the PMM8650AU/PMM8620AU must be enabled by the SoC software. See the latest revision of the applicable software release notes to identify the enabled PMM8650AU/PMM8620AU features.

Table 1-1 PMM8650AU/PMM8620AU features

Feature	PMM8650AU/PMM8620AU capability
System architecture	
Main domain	Power management General housekeeping GPIOs Clock generation and output Power on/off control
Real-time (RTSS) domain	Real-time monitoring Fault detection and fault aggregator Data storage and event logging
Input power management	
Coin cell or capacitor backup	Keep-alive power source
Output voltage regulation	
Switched-mode power supplies FT-SMPS	Nine
Low-dropout linear regulators	Nine
General housekeeping	
On-chip ADC	Shared housekeeping (HK) and XO support
Analog multiplexing for ADC	
HK inputs	Many internal nodes and external inputs
Overtemperature protection	Multistage smart thermal control
38.4 MHz oscillator support	XO (with on-chip ADC)
XO outputs	Three low-noise baseband outputs
Special purpose clock outputs	Sleep clock; 19.2, 9.6, 4.8, 2.4, and 1.2 MHz, including low-power mode one high-speed GPIO for fast clocks
Real-time clock (RTC)	RTC circuits and alarms
IC-level interfaces	
Primary status and control	Two-line SPMI
Interrupt managers	Supported by SPMI
Power sequencing	Power-on, power-off, and soft resets
Functional safety status and control	Two-line I^{2}C
Configurable I/Os	
GPIO pins	12; configurable as digital inputs or outputs or analog pass-through
Analog multiplexer (AMUX) pins	Six ADC inputs
Package	

Table 1-1 PMM8650AU/PMM8620AU features (cont.)

Feature	PMM8650AU/PMM8620AU capability
Size	9.30 × 9.30 × 1.18 mm
Pin count and package type	MSP181

2 Pin definitions

2.1 I/O parameter definitions

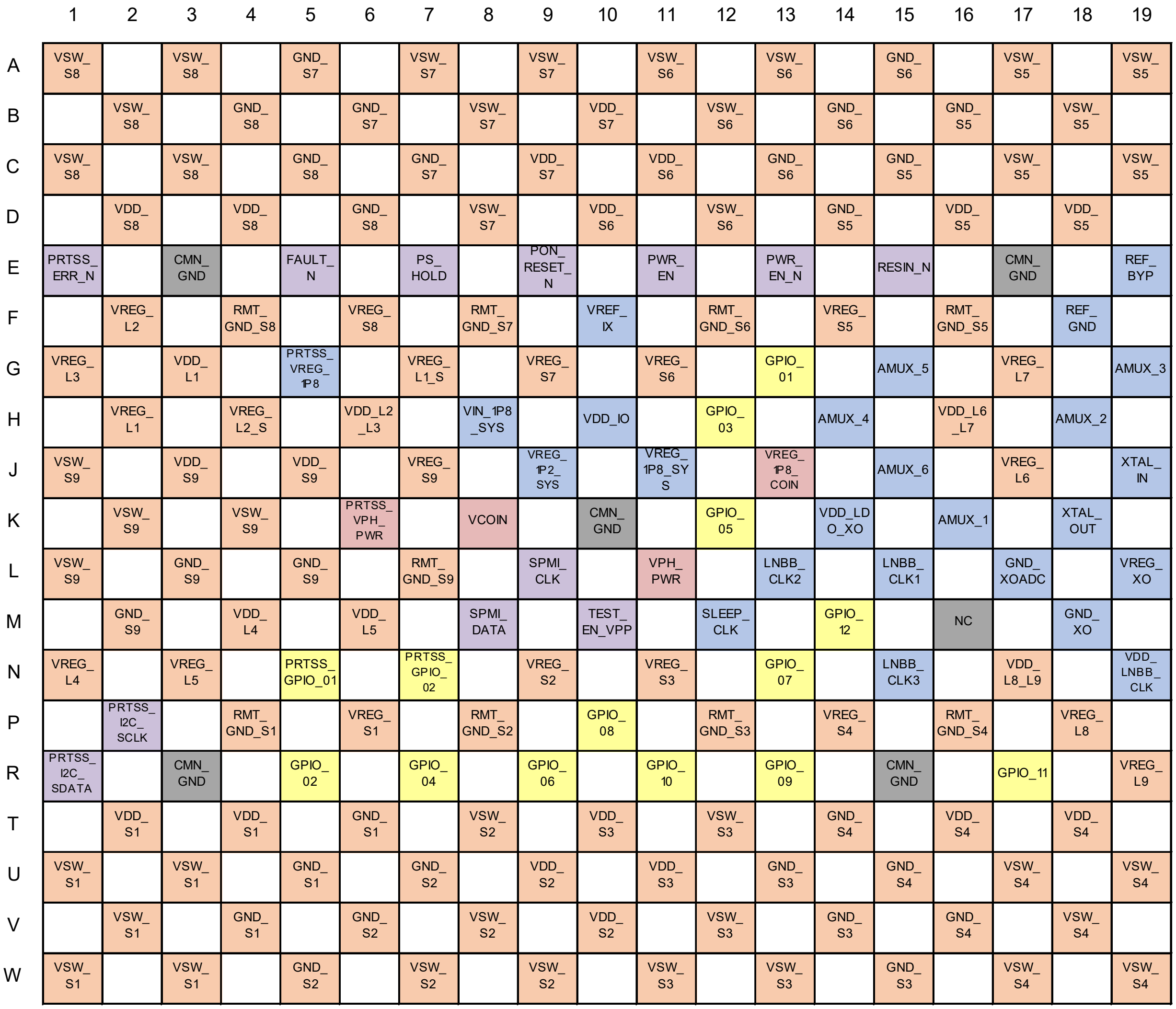
Table 2-1 I/O parameter (pad type) definitions

Symbol	Definition
Pad attribute	
AI	Analog input
AO	Analog output
DI	Digital input (CMOS)
DO	Digital output (CMOS)
PI	Power input; a pin that handles 10 mA or more of current flow into the device
PO	Power output; a pin that handles 10 mA or more of current flow out of the device
Z	High-impedance (Hi-Z) output
MV	Medium voltage (1.8 V or VPH_PWR)
LV	Low voltage (1.8 V only)
GNDP	Power ground; a pad that handles 10 mA or more of current flow returning to ground. Layout considerations must be made for these pads
GNDC	Common ground; a pad that does not handle a significant amount of current flow, typically used for grounding digital circuits and substrates
Pad voltage groupings	
V_INT	Internally generated supply voltage for some power-on circuits
V_PAD	Supply for SoC IC interfaces
V_XBB	Supply for LN_BB_CLKx output buffer
V_XRF	Supply for RF_CLKx output buffers
GPIO pin configurations	
When configured as inputs, GPIO pins have configurable pull settings.	
NP	No internal pull enabled
PU	Internal pull-up enabled
PD	Internal pull-down enabled
When configured as outputs, GPIO pins have configurable drive strengths that depend on the GPIO pad’s supply voltage. See Electrical specifications for details.	

2.2 Pin assignments

The PMM8650AU/PMM8620AU is available in the 181 MSP. See Mechanical information for package details.

A high-level view of the pin assignments is shown in Figure 2-1.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	VSW_S8		VSW_S8		GND_S7		VSW_S7		VSW_S7		VSW_S6		VSW_S6		GND_S6		VSW_S5		VSW_S5
B		VSW_S8		GND_S8		GND_S7		VSW_S7		VDD_S7		VSW_S6		GND_S6		GND_S5		VSW_S5	
C	VSW_S8		VSW_S8		GND_S8		GND_S7		VDD_S7		VDD_S6		GND_S6		GND_S5		VSW_S5		VSW_S5
D		VDD_S8		VDD_S8		GND_S8		VSW_S7		VDD_S6		VSW_S6		GND_S5		VDD_S5		VDD_S5	
E	PRTSS_ERR_N		CMN_GND		FAULT_N		PS_HOLD		PON_RESET_N		PWR_EN		PWR_EN_N		RESIN_N		CMN_GND		REF_BYP
F		VREG_L2		RMT_GND_S8		VREG_S8		RMT_GND_S7		VREF_IX		RMT_GND_S6		VREG_S5		RMT_GND_S5		REF_GND	
G	VREG_L3		VDD_L1		PRTSS_VREG_1P8		VREG_L1_S		VREG_S7		VREG_S6		GPIO_01		AMUX_5		VREG_L7		AMUX_3
H		VREG_L1		VREG_L2_S		VDD_L2_L3		VIN_1P8_SYS		VDD_IO		GPIO_03		AMUX_4		VDD_L6_L7		AMUX_2	
J	VSW_S9		VDD_S9		VDD_S9		VREG_S9		VREG_1P2_SYS		VREG_1P8_SYS		VREG_1P8_COIN		AMUX_6		VREG_L6		XTAL_IN
K		VSW_S9		VSW_S9		PRTSS_VPH_PWR		VCOIN		CMN_GND		GPIO_05		VDD_LDO_XO		AMUX_1		XTAL_OUT	
L	VSW_S9		GND_S9		GND_S9		RMT_GND_S9		SPMI_CLK		VPH_PWR		LNBB_CLK2		LNBB_CLK1		GND_XOADC		VREG_XO
M		GND_S9		VDD_L4		VDD_L5		SPMI_DATA		TEST_EN_VPP		SLEEP_CLK		GPIO_12		NC		GND_XO	
N	VREG_L4		VREG_L5		PRTSS_GPIO_01		PRTSS_GPIO_02		VREG_S2		VREG_S3		GPIO_07		LNBB_CLK3		VDD_L8_L9		VDD_LNBB_CLK
P		PRTSS_I2C_SCLK		RMT_GND_S1		VREG_S1		RMT_GND_S2		GPIO_08		RMT_GND_S3		VREG_S4		RMT_GND_S4		VREG_L8	
R	PRTSS_I2C_SDATA		CMN_GND		GPIO_02		GPIO_04		GPIO_06		GPIO_10		GPIO_09		CMN_GND		GPIO_11		VREG_L9
T		VDD_S1		VDD_S1		GND_S1		VSW_S2		VDD_S3		VSW_S3		GND_S4		VDD_S4		VDD_S4	
U	VSW_S1		VSW_S1		GND_S1		GND_S2		VDD_S2		VDD_S3		GND_S3		GND_S4		VSW_S4		VSW_S4
V		VSW_S1		GND_S1		GND_S2		VSW_S2		VDD_S2		VSW_S3		GND_S3		GND_S4		VSW_S4	
W	VSW_S1		VSW_S1		GND_S2		VSW_S2		VSW_S2		VSW_S3		VSW_S3		GND_S3		VSW_S4		VSW_S4

Figure 2-1 PMM8650AU/PMM8620AU pin assignments (top view)

2.2.1 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

Table 2-2 Input power management

Table 2-3 Output power management

Table 2-4 General housekeeping

Table 2-5 IC-level interfaces

Table 2-6 General-purpose input/output: Primary PMIC PMM8620AU GPIO table for QCS8275

Table 2-7 General-purpose input/output: Secondary PMIC PMM8650AU GPIO table for QCS8275

Table 2-8 General-purpose input/output: Primary PMIC PMM8620AU GPIO table for QCS8300

Table 2-9 General-purpose input/output: Secondary PMIC PMM8650AU GPIO table for QCS8300

Table 2-10 General-purpose input/output: Primary A PMIC PMM8650AU-4 GPIO table for QCS8300

Table 2-11 General-purpose input/output: Secondary C PMIC PMM8650AU-0 GPIO table for QCS8300

Table 2-12 General-purpose input/output: Secondary E PMIC PMM8650AU-0 GPIO table for QCS8300

Table 2-13 General-purpose input/output: Secondary G PMIC PMM8650AU-0 GPIO table for QCS8300

Table 2-14 No connection pins

Table 2-15 Common ground pins

Table 2-2 Pin descriptions – input power management functions

Pin #	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
Input power sources				
L11	VPH_PWR	MV	PI	System input power node generated by an external 3.3 V power supply
J13	VREG_1P8_COIN	LV	PI	Output cap for VCOIN regulator
K8	VCOIN	MV	PI	VCOIN power input
K6	PRTSS_VPH_PWR	MV	PI	Input power for PRTSS

[a] See Table 2-1 for pin voltage and type definitions.

Table 2-3 Pin descriptions – output power management functions

Pin #	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
Fast-transient buck SMPS circuits				
U1, W1, U3, W3, V2	VSW_S1	MV	PO	S1 SMPS switch node
P6	VREG_S1	LV	AI	S1 SMPS sense input
P4	RMT_GND_S1	GND	GND	Remote ground sense at the SoC
T2, T4	VDD_S1	MV	PI	S1 SMPS supply power input
U5, V4, T6	GND_S1	GND	GND	Switching ground for VREG_S1
W7, W9, T8, V8	VSW_S2	MV	PO	S2 SMPS switch node
N9	VREG_S2	LV	AI	S2 SMPS sense input
P8	RMT_GND_S2	GND	GND	Remote ground sense at the SoC

Table 2-3 Pin descriptions – output power management functions (cont.)

Pin #	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
U9, V10	VDD_S2	MV	PI	S2 SMPS supply power input
W5, U7, V6	GND_S2	GND	GND	Switching ground for VREG_S2
W11, W13, T12, V12	VSW_S3	MV	PO	S3 SMPS switch node
N11	VREG_S3	LV	AI	S3 SMPS sense input
P12	RMT_GND_S3	GND	GND	Remote ground sense at the SoC
U11, T10	VDD_S3	MV	PI	S3 SMPS supply power input
U13, W15, V14	GND_S3	GND	GND	Switching ground for VREG_S3
U17, W17, U19, W19, V18	VSW_S4	MV	PO	S4 SMPS switch node
P14	VREG_S4	LV	AI	S4 SMPS sense input
P16	RMT_GND_S4	GND	GND	Remote ground sense at the SoC
T16, T18	VDD_S4	MV	PI	S4 SMPS supply power input
U15, T14, V16	GND_S4	GND	GND	Switching ground for VREG_S4
A17, C17, A19, C19, B18	VSW_S5	MV	PO	S5 SMPS switch node
F14	VREG_S5	LV	AI	S5 SMPS sense input
F16	RMT_GND_S5	GND	GND	Remote ground sense at the SoC
D16, D18	VDD_S5	MV	PI	S5 SMPS supply power input
C15, D14, B16	GND_S5	GND	GND	Switching ground for VREG_S5
A11, A13, B12, D12	VSW_S6	MV	PO	S6 SMPS switch node
G11	VREG_S6	LV	AI	S6 SMPS sense input
F12	RMT_GND_S6	GND	GND	Remote ground sense at the SoC
C11, D10	VDD_S6	MV	PI	S6 SMPS supply power input
C13, A15, B14	GND_S6	GND	GND	Switching ground for VREG_S6
A7, A9, B8, D8	VSW_S7	MV	PO	S7 SMPS switch node
G9	VREG_S7	LV	AI	S7 SMPS sense input
F8	RMT_GND_S7	GND	GND	Remote ground sense at the SoC
C9, B10	VDD_S7	MV	PI	S7 SMPS supply power input
A5, C7, B6	GND_S7	GND	GND	Switching ground for VREG_S7
A1 ,C1 ,A3 ,C3 ,B2	VSW_S8	MV	PO	S8 SMPS switch node
F6	VREG_S8	LV	AI	S8 SMPS sense input
F4	RMT_GND_S8	GND	GND	Remote ground sense at the SoC
D2, D4	VDD_S8	MV	PI	S8 SMPS supply power input
C5, B4, D6	GND_S8	GND	GND	Switching ground for VREG_S8
J1, L1, K2, K4	VSW_S9	MV	PO	S9 SMPS switch node
J7	VREG_S9	LV	AI	S9 SMPS sense input
L7	RMT_GND_S9	GND	GND	Remote ground sense at the SoC
J3, J5	VDD_S9	MV	PI	S9 SMPS supply power input
L3, L5, M2	GND_S9	GND	GND	Switching ground for VREG_S9

Table 2-3 Pin descriptions – output power management functions (cont.)

Pin #	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
Low dropout regulator (LDO) circuits				
H2	VREG_L1	LV	PO	L1 LDO regulated output
G7	VREG_L1_S	LV	AI	L1 sense input
F2	VREG_L2	LV	PO	L2 LDO regulated output
H4	VREG_L2_S	LV	AI	L2 sense input
G1	VREG_L3	LV	PO	L3 LDO regulated output
N1	VREG_L4	LV	PO	L4 LDO regulated output
N3	VREG_L5	LV	PO	L5 LDO regulated output
J17	VREG_L6	LV	PO	L6 LDO regulated output
G17	VREG_L7	LV	PO	L7 LDO regulated output
P18	VREG_L8	LV	PO	L8 LDO regulated output
R19	VREG_L9	LV	PO	L9 LDO regulated output
G3	VDD_L1	LV	PI	LDO input
H6	VDD_L2_L3	LV	PI	LDO input
M4	VDD_L4	LV	PI	LDO input
M6	VDD_L5	LV	PI	LDO input
H16	VDD_L6_L7	LV	PI	LDO input
N17	VDD_L8_L9	MV	PI	LDO input

[a] See Table 2-1 for pin voltage and type definitions.

Table 2-4 Pin descriptions – general housekeeping functions

Pin #	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
Analog multiplexer and HK/XO ADC circuits				
K16	AMUX_1	LV	AI	Analog multiplexer (AMUX) input
H18	AMUX_2	LV	AI	Analog multiplexer (AMUX) input
G19	AMUX_3	LV	AI	Analog multiplexer (AMUX) input
H14	AMUX_4	LV	AI	Analog multiplexer (AMUX) input
G15	AMUX_5	LV	AI	Analog multiplexer (AMUX) input
J15	AMUX_6	LV	AI	Analog multiplexer (AMUX) input
L17	GND_XOADC	GND	GND	XO ADC reference ground
H10	VDD_IO	LV	PI	Input for IO voltage reference
K14	VDD_LDO_XO	LV	PI	Input for XO LDO
N19	VDD_LNBB_CLK	LV	PI/PO	LNBB_CLK buffer. Output for PMM8650AU/PMM8620AU, input for PMAU0101.
H8	VIN_1P8_SYS	LV	PI	Input for high power 1p8 sys regulator
E19	REF_BYP	LV	AO	Bandgap reference
F18	REF_GND	GND	GND	Bandgap reference ground

Table 2-4 Pin descriptions – general housekeeping functions (cont.)

Pin #	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
Crystal oscillator (XO) circuits and buffered outputs				
J19	XTAL_IN	LV	AI	38.4 MHz oscillator
K18	XTAL_OUT	LV	AO	38.4 MHz oscillator output
L19	VREG_XO	LV	PO	XO VREG (internal use only), capacitor installed internally
M18	GND_XO	GND	GND	Ground for 38.4 MHz XO
J9	VREG_1P2_SYS	LV	PO	Output for system 1.2 V reference voltage
J11	VREG_1P8_SYS	LV	PO	Output for system 1.8 V reference voltage
L15	LNBB_CLK1	LV	DO	Low noise baseband clock output 1
L13	LNBB_CLK2	LV	DO	Low noise baseband clock output 2
N15	LNBB_CLK3	LV	DO	Low noise baseband clock output 3
G5	PRTSS_VREG_1P8	LV	PO	Output for PRTSS 1.8 V reference voltage
Sleep clock				
M12	SLEEP_CLK	LV	DO	32 kHz sleep-clock output
Vref outputs				
F10	VREF_IX	LV	AO	General reference voltage source 0.85 V (default) or 1.25 V
GPIOs can be configured for general housekeeping functions not listed here. [b]				

[a] See Table 2-1 for pin voltage and type definitions.
[b] Other IC-level interface GPIO functions are possible. To assign a GPIO a particular function, identify all of your application's requirements and map each GPIO to its function, carefully avoiding assignment conflicts. All GPIOs are listed in Table 2-6.

Table 2-5 Pin descriptions – IC-level interface functions

Pin #	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
Power-on/power-off/reset control				
E5	FAULT_N	LV	DI, DO	PMIC fault signal (bidirectional 200 kΩ [b] internal PU 1.8 V only that initiates shutdown or S3 reset to all PMICs. No external circuitry should be connected to this pin)
E9	PON_RESET_N	LV	DO	Reset output to SoC device's RESIN_N (1.8 V or 1.2 V depending on chipset IO voltage)
E7	PS_HOLD	LV	DI	Power supply hold
E1	PRTSS_ERR_N	LV	DO	PMIC PRTSS domain error signal active low. Indicates PMIC error and resulting PMIC shutdown. Connect to MCU for monitoring purpose.
E13	PWR_EN_N	LV/MV	DI	Power-on trigger active-low; 200 kΩ internal PU to 1.8 V, but will only measure ~0.8 V for 1.8 V PU at the pin due to internal series FET.
E15	RESIN_N	LV/MV	DI	Reset input; 40 kΩ [b] internal 1.8 V PU, but will only measure ~0.8 V for 1.8 V PU at the pin due to internal series FET.
E11	PWR_EN	LV/MV	DI	Power-on trigger active-high (200 kΩ internal pull-down to GND)
System power management interface (SPMI)/Inter-IC bus (I^2C) signals				
L9	SPMI_CLK	LV	DI, DO	SPMI communication bus clock signal (1.8 V or 1.2 V depending on chipset IO voltage)
M8	SPMI_DATA	LV	DI, DO	SPMI data (1.8 V or 1.2 V depending on chipset IO voltage)

Table 2-5 Pin descriptions – IC-level interface functions (cont.)

Pin #	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
P2	PRTSS_I2C_SCLK	LV	DI, DO	I^2C clock
R1	PRTSS_I2C_SDATA	LV	DI, DO	I^2C data
Miscellaneous IC functions				
M10	TEST_EN_VPP	MV	DI	Pin must be grounded externally
GPIOs can be configured for IC-level interface functions not listed here [c]				

[a] See Table 2-1 for pin voltage and type definitions.
[b] Value is ± 25% over ambient operating temperature.
[c] Other IC-level interface GPIO functions are possible. To assign a GPIO a particular function, identify all of your application's requirements and map each GPIO to its function, carefully avoiding assignment conflicts. All GPIOs are listed in Table 2-6.

Table 2-6 Pin descriptions – general-purpose input/output functions: Primary PMIC PMM8620AU GPIO table for QCS8275

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
G13	GPIO_01	LV	DS_EN: Indicates to SoC that PMIC is in deep sleep
R5	GPIO_02	MV	POFF_COMPLETE_N: indicates the status of power-on or power-off completion of PMM8620AUs Transition from Low to High: Power-on sequence is completed Transition from High to Low: Power-off sequence is completed
H12	GPIO_03	MV	UFS0_VER_IND: UFS0 version detection Logic high or HIG-Z: UFS 3.x Logic low: UFS 2.1/EMMC
R7	GPIO_04	MV	FAST_POFF_EN_N: interrupt to initiate a fast power off sequence on PMM8620AUs, active low input, internal pull up to 3.3 V by default
K12	GPIO_05	MV	Spare
R9	GPIO_06	MV	AOSS_SLEEP_ENTRY_EXIT: indicates SoC sleep state entry or exit Logic high: sleep entry Logic low: sleep exit
N13	GPIO_07	MV	Spare
P10	GPIO_08	MV	Spare
R13	GPIO_09	MV	USB0_PWR_EN_3P3: USB0 3.3 V Power Enable
R11	GPIO_10	MV	USB0_FAULT_3P3_N: USB0 Fault 3.3 V
R17	GPIO_11	MV	UEFI_BTN_3P3_N: SoC Boot Option
M14	GPIO_12	MV	OPTION: Analog PON option
N5	PRTSS_GPIO_01	LV	GPIO reserved for PRTSS use
N7	PRTSS_GPIO_02	MV	GPIO reserved for PRTSS use

[a] See Table 2-1 for pin voltage and type definitions.

Table 2-7 Pin descriptions – general-purpose input/output functions: Secondary PMIC PMM8650AU GPIO table for QCS8275

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
G13	GPIO_01	LV	Spare
R5	GPIO_02	MV	Spare
H12	GPIO_03	MV	Spare
R7	GPIO_04	MV	WLAN_DBU3_EN
K12	GPIO_05	MV	Spare
R9	GPIO_06	MV	WLAN_DBU4_EN
N13	GPIO_07	MV	USB1_PWR_EN_3P3: USB1 3.3 V Power Enable
P10	GPIO_08	MV	USB1_FAULT_3P3_N: USB1 Fault 3.3 V
R13	GPIO_09	MV	Spare
R11	GPIO_10	MV	Spare
R17	GPIO_11	MV	VMON_MD_VDD_QFPROM: Main Domain VDD_QFPROM Monitor (VREG_L9C)
M14	GPIO_12	MV	Spare
N5	PRTSS_GPIO_01	LV	GPIO reserved for PRTSS use
N7	PRTSS_GPIO_02	MV	GPIO reserved for PRTSS use

[a] See Table 2-1 for pin voltage and type definitions.

Table 2-8 Pin descriptions – general-purpose input/output functions: Primary PMIC PMM8620AU GPIO table for QCS8300

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
G13	GPIO_01	LV	DS_EN: Indicates to SoC that PMIC is in deep sleep
R5	GPIO_02	MV	POFF_COMPLETE_N: indicates the status of power-on or power-off completion of PMM8620AUs Transition from Low to High: Power-on sequence is completed Transition from High to Low: Power-off sequence is completed
H12	GPIO_03	MV	UFS0_VER_IND: UFS0 version detection Logic high or HIG-Z: UFS 3.x Logic low: UFS 2.1/EMMC
R7	GPIO_04	MV	FAST_POFF_EN_N: interrupt to initiate a fast power off sequence on PMM8620AUs, active low input, internal pull up to 3.3 V by default
K12	GPIO_05	MV	PRTSS_PMIC_PON_DONE: Indicates that PRTSS PMIC has completed PON
R9	GPIO_06	MV	AOSS_SLEEP_ENTRY_EXIT: indicates SoC sleep state entry or exit Logic High: sleep entry Logic Low: sleep exit
N13	GPIO_07	MV	PRTSS_S2_PMIC_EN: PRTSS PMIC Enable for Buck 2
P10	GPIO_08	MV	PRTSS_S2_PGOOD: PRTSS PMIC Power Good For Buck 2
R13	GPIO_09	MV	USB0_PWR_EN_3P3: USB0 3.3 V Power Enable

Table 2-8 Pin descriptions – general-purpose input/output functions: Primary PMIC PMM8620AU GPIO table for QCS8300 (cont.)

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
R11	GPIO_10	MV	USB0_FAULT_3P3_N: USB0 Fault 3.3 V
R17	GPIO_11	MV	UEFI_BTN_3P3_N: SoC Boot Option
M14	GPIO_12	MV	OPTION: Analog PON option
N5	PRTSS_GPIO_01	LV	GPIO reserved for PRTSS use
N7	PRTSS_GPIO_02	MV	GPIO reserved for PRTSS use

[a] See Table 2-1 for pin voltage and type definitions.

Table 2-9 Pin descriptions – general-purpose input/output functions: Secondary PMIC PMM8650AU GPIO table for QCS8300

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
G13	GPIO_01	LV	Spare
R5	GPIO_02	MV	Spare
H12	GPIO_03	MV	Spare
R7	GPIO_04	MV	Spare
K12	GPIO_05	MV	PRTSS PMIC-S2S Buck LPM trigger. (High: LPM, Low: NPM)
R9	GPIO_06	MV	Spare
N13	GPIO_07	MV	USB1_PWR_EN_3P3: USB1 3.3 V power enable
P10	GPIO_08	MV	USB1_FAULT_3P3_N: USB1 fault 3.3 V
R13	GPIO_09	MV	Spare
R11	GPIO_10	MV	Spare
R17	GPIO_11	MV	VMON_MD_VDD_QFPROM: Main Domain VDD_QFPROM Monitor (VREG_L9C)
M14	GPIO_12	MV	Spare
N5	PRTSS_GPIO_01	LV	GPIO reserved for PRTSS use
N7	PRTSS_GPIO_02	MV	GPIO reserved for PRTSS use

[a] See Table 2-1 for pin voltage and type definitions.

Table 2-10 Pin descriptions – general-purpose input/output functions: Primary A PMIC PMM8650AU-4 GPIO table for QCS9075

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
G13	GPIO_01	LV	DS_EN: Indicates to SoC that PMIC is in deep sleep
R5	GPIO_02	MV	POFF_COMPLETE_N: indicates the status of power-on or power-off completion of PMM8650AUs Transition from low to high: Power-on sequence is completed Transition from high to low: Power-off sequence is completed

Table 2-10 Pin descriptions – general-purpose input/output functions: Primary A PMIC PMM8650AU-4 GPIO table for QCS9075 (cont.)

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
H12	GPIO_03	MV	UFS0_VER_IND: UFS0 version detection Logic high or HIG-Z: UFS 3.x Logic low: UFS 2.1/EMMC. Internal pull up to 3.3 V by default
R7	GPIO_04	MV	FAST_POFF_EN_N: interrupt to initiate a fast power off sequence on PMM8650AUs, active low input, internal pull up to 3.3 V by default
K12	GPIO_05	MV	Spare
R9	GPIO_06	MV	AOSS_SLEEP_ENTRY_EXIT: indicates SoC sleep state entry or exit Logic high: sleep entry Logic low: sleep exit
N13	GPIO_07	MV	Spare
P10	GPIO_08	MV	Spare
R13	GPIO_09	MV	Spare
R11	GPIO_10	MV	Spare
R17	GPIO_11	MV	UEFI_BTN_3P3_N: SoC boot option
M14	GPIO_12	MV	OPTION: Analog PON option
N5	PRTSS_GPIO_01	LV	GPIO reserved for PRTSS use
N7	PRTSS_GPIO_02	MV	GPIO reserved for PRTSS use

[a] See Table 2-1 for pin voltage and type definitions.

Table 2-11 Pin descriptions – general-purpose input/output functions: Secondary C PMIC PMM8650AU-0 GPIO table for QCS9075

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
G13	GPIO_01	LV	GND. Must be grounded for C PMIC option pin decode
R5	GPIO_02	MV	GND. Must be grounded for C PMIC option pin decode
H12	GPIO_03	MV	UFS1_VER_IND: UFS1 version detection Logic high or HIG-Z: UFS 3.x Logic low: UFS 2.1/EMMC. Internal pull up to 3.3 V by default
R7	GPIO_04	MV	Spare
K12	GPIO_05	MV	Spare
R9	GPIO_06	MV	Spare
N13	GPIO_07	MV	Spare
P10	GPIO_08	MV	Spare
R13	GPIO_09	MV	Spare
R11	GPIO_10	MV	Spare
R17	GPIO_11	MV	Spare

Table 2-11 Pin descriptions – general-purpose input/output functions: Secondary C PMIC PMM8650AU-0 GPIO table for QCS9075 (cont.)

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
M14	GPIO_12	MV	Spare
N5	PRTSS_GPIO_01	LV	GPIO reserved for PRTSS use
N7	PRTSS_GPIO_02	MV	GPIO reserved for PRTSS use

[a] See Table 2-1 for pin voltage and type definitions.

Table 2-12 Pin descriptions – general-purpose input/output functions: Secondary E PMIC PMM8650AU-0 GPIO table for QCS9075

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
G13	GPIO_01	LV	No connect. Must be left floating for G PMIC option pin decode
R5	GPIO_02	MV	GND. Must be grounded for G PMIC option pin decode
H12	GPIO_03	MV	Spare
R7	GPIO_04	MV	Spare
K12	GPIO_05	MV	Spare
R9	GPIO_06	MV	Spare
N13	GPIO_07	MV	Spare
P10	GPIO_08	MV	Spare
R13	GPIO_09	MV	Spare
R11	GPIO_10	MV	Spare
R17	GPIO_11	MV	Spare
M14	GPIO_12	MV	VMON_PRTSS_PX8
N5	PRTSS_GPIO_01	LV	GPIO reserved for PRTSS use
N7	PRTSS_GPIO_02	MV	GPIO reserved for PRTSS use

[a] See Table 2-1 for pin voltage and type definitions.

Table 2-13 Pin descriptions – general-purpose input/output functions: Secondary G PMIC PMM8650AU-0 GPIO table for QCS9075

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
G13	GPIO_01	LV	GND. Must be grounded for for option pin decode
R5	GPIO_02	MV	No connect. Must be left floating for G PMIC option pin decode
H12	GPIO_03	MV	Spare
R7	GPIO_04	MV	Spare
K12	GPIO_05	MV	Spare
R9	GPIO_06	MV	Spare

Table 2-13 Pin descriptions – general-purpose input/output functions: Secondary G PMIC PMM8650AU-0 GPIO table for QCS9075 (cont.)

Pin #	Pin name	Pin characteristics [a]	Functional description
		Voltage	
N13	GPIO_07	MV	Spare
P10	GPIO_08	MV	Spare
R13	GPIO_09	MV	Spare
R11	GPIO_10	MV	Spare
R17	GPIO_11	MV	Spare
M14	GPIO_12	MV	Spare
N5	PRTSS_GPIO_01	LV	GPIO reserved for PRTSS use
N7	PRTSS_GPIO_02	MV	GPIO reserved for PRTSS use

[a] See Table 2-1 for pin voltage and type definitions.

Table 2-14 Pin descriptions – no connection pins

Pin #	Pin name	Pin characteristics		Functional description
		Voltage	Type	
No connection pins				
M16	NC	0	–	Not connected

Table 2-15 Pin descriptions – common grounds

Pin #	Pin name	Pin characteristics [a]		Functional description
		Voltage	Type	
Common ground				
E3	CMN_GND	GND	GND	Ground for all non-specialized circuits
R3	CMN_GND	GND	GND	Ground for all non-specialized circuits
R15	CMN_GND	GND	GND	Ground for all non-specialized circuits
E17	CMN_GND	GND	GND	Ground for all non-specialized circuits
K10	CMN_GND	GND	GND	Ground for all non-specialized circuits

[a] See Table 2-1 for pin voltage and type definitions.

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings shown in the following table reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Operating conditions.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Units
Power supply pads				
VPH_PWR	Main power-supply voltage	-0.5	+6	V
VDD_xxx	PMIC power-supply voltages not listed elsewhere (steady state)	-0.5	+6	V
	Transient (< 10 ms)	-0.5	+7	V
GPIO_xx	MV	-0.5	6	V
	LV	-0.5	2.2	V
T_S	Storage temperature [a] [b]	-65	150	°C
T_J	Junction temperature	-55	155	°C
ESD protection and thermal conditions – see Part reliability and Thermal characteristics				

[a] The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.

[b] For devices shipped in tape and reel, the storage temperature range is [+15°C~35°C] and < -90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

The PMM8650AU/PMM8620AU meets all performance specifications, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded)

Table 3-2 Operating conditions

Parameter		Min	Typ	Max	Units
Power supply pads					
VPH_PWR	Main power-supply voltage (steady state)	+3.1	+3.3	+3.5	V
VPH_PWR	Main power-supply voltage (< 1 ms transient)	+3.0	+3.3	+3.6	V
VDD_xxx [a]	All power supply pads not otherwise listed in this table (xxx is defined in Pin definitions)	+3.1	+3.3	+3.5	V
VCOIN		+2.5	+3.3	+3.5	V
GPIO_xx	MV	–	VPH	–	V
	LV	–	1.8	–	V
Signal pins					
V_IN	Voltage on any nonpower-supply pin [b]	0	–	V_{XX} + 0.5	V
Thermal conditions					

Table 3-2 Operating conditions (cont.)

Parameter		Min	Typ	Max	Units
T_A	Ambient operating temperature	-40	+25	+105	°C
T_J	Junction operating temperature	–	–	+125	°C

[a] 3.1 V to 3.5 V is the operating range for full specification compliance except for high VOUT LDOs where VPH does not meet headroom requirement. System shall ensure that LDO performance with compressed headroom meets system requirements.

[b] V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.3 DC power consumption

This section specifies DC power supply currents for the various IC operating modes (Table 3-3). Typical currents are based on IC operation at room temperature (+25°C) using default settings.

Table 3-3 DC power supply currents

Parameter		Condition	Min	Typ	Max	Units
I_OFF	Supply current, off mode [a]	3.3 V input supply current, off mode	–	100	650	µA
I_COIN	Supply current, off mode, RC calibration [b]	Average current	–	42	450	µA

[a] I_OFF is the supply current from the 3.3 V PMIC input for one PMIC with the PMIC off (all regulators off).

[b] I_COIN is the supply current from the coin cell of one PMIC with the PMIC off (all regulators off).

3.4 PMM8650AU/PMM8620AU output power management

Output power management circuits include:

- PMM8650AU/PMM8620AU fast-transient switched mode power supply (FTS527) circuits
- PMM8650AU/PMM8620AU LDO linear (LDO515) regulators
- PMM8650AU/PMM8620AU LDO linear (LDO512) regulator

NOTE Current ratings and voltage values in all the below tables, are not final and are subject to change.

Table 3-4 QCS8275 Primary PMIC (PMM8620AU-2) SMPS regulator summary

Regulator	Circuit type	I_{rated} (mA)	Transient load step rating (A)/phase	Default booting voltage (V)
S1A	FTS527	6000	2/100 nS	0.968
S2A	FTS527	6000	2/100 nS	0.968
S4A	FTS527	3500	2/100 nS	1.8
S5A	FTS527	6000	2/100 nS	0.888
S6A	FTS527	6000	2/100 nS	0.888
S7A_8A	FTS527	12000	2/100 nS	0.968
S9A	FTS527	3500	2/100 nS	1.352

Table 3-5 QCS8275 Secondary PMIC (PMM8650AU-0/PMM8620AU-0) SMPS regulator summary

Regulator	Circuit type	I_{rated} (mA)	Transient load step rating (A)/phase	Default booting voltage (V)
S1C	FTS527	6000	2/100 nS	0.952
S2C_3C	FTS527	12000	2/100 nS	0.968
S4C	FTS527	6000	2/100 nS	0.968

Table 3-5 QCS8275 Secondary PMIC (PMM8650AU-0/PMM8620AU-0) SMPS regulator summary (cont.)

Regulator	Circuit type	I_{rated} (mA)	Transient load step rating (A)/phase	Default booting voltage (V)
S5C	FTS527	6000	2/100 nS	1.1
S6C_7C_8C	FTS527	18000	2/100 nS	0.968
S9C	FTS527	6000	2/100 nS	0.968

Table 3-6 QCS8275 Primary PMIC (PMM8620AU-2), Secondary PMIC (PMM8650AU-0/PMM8620AU-0) LDO regulator summary

Regulator	Circuit type	I_{rated} (mA)	PMM8620AU-2 (Primary PMIC) Default booting voltage (V)	PMM8650AU-0/PMM8620AU-0 (Secondary PMIC) Default booting voltage (V)
L1	LDO515 LV NMOS 1200	1200	0.888	0.5
L2	LDO515 LV NMOS 1200	1200	0.968	0.9
L3	LDO515 LV NMOS 300	300	1.2	–
L4	LDO515 LV NMOS 1200	1200	0.88	1.2
L5	LDO515 LV NMOS 1200	1200	1.2	–
L6	LDO515 LV NMOS 1200	1200	0.912	1.8
L7	LDO515 LV NMOS 300	300	0.88	1.8
L8	LDO515 MV PMOS 1200	1200	2.96	1.8
L9	LDO512 MV PMOS 150	150	3.072	1.8

Table 3-7 QCS8300 Primary PMIC (PMM8620AU-2) SMPS regulator summary

Regulator	Circuit type	I_{rated} (mA)	Transient load step rating (A)/phase	Default booting voltage (V)
S9A_1A	FTS527	12000	2/100 nS	0.968
S2A_3A_4A	FTS527	13000	2/100 nS	0.968
S5A	FTS527	6000	2/100 nS	0.888
S6A	FTS527	6000	2/100 nS	0.888
S7A_8A	FTS527	12000	2/100 nS	0.968

Table 3-8 QCS8300 Secondary PMIC (PMM8650AU-0/PMM8620AU-0) SMPS regulator summary

Regulator	Circuit type	I_{rated} (mA)	Transient load step rating (A)/phase	Default booting voltage (V)
S1C	FTS527	6000	2/100 nS	0.952
S2C_3C	FTS527	12000	2/100 nS	0.968
S4C	FTS527	6000	2/100 nS	0.968
S5C	FTS527	6000	2/100 nS	1.1
S6C_7C_8C	FTS527	18000	2/100 nS	0.968
S9C	FTS527	3500	2/100 nS	1.352

Table 3-9 QCS9075 A PMIC (PMM8650AU-4) SMPS regulator summary

Regulator	Circuit type	Irated (A)	Transient load step rating (A/100 ns)	Default booting voltage (V)
S1A_S2A_S3A	FTS527	18	2	0.824
S4A		4	1	1.8
S5A		3	1	1.95
S6A_S7A_S8A		18	2	0.824
S9A		6	1	1

Table 3-10 QCS9075 C PMIC (PMM8650AU-0) SMPS regulator summary

Regulator	Circuit type	Irated (A)	Transient load step rating (A/100 ns)	Default booting voltage (V)
S1C_S2C	FTS527	12	2	0.824
S3C_S4C		12	2	0.824
S5C		6	2	0.824
S6C_S7C_S8C_S9C		24	2	0.824

Table 3-11 QCS9075 E PMIC (PMM8650AU-0) SMPS regulator summary

Regulator	Circuit type	Irated (A)	Transient load step rating (A/100 ns)	Default booting voltage (V)
S1E_S2E_S3E	FTS527	18	2	0.824
S4E		6	1	1.352
S5E_S6E		12	2	0.824
S7E		6	2	1.1
S8E		6	2	0.952
S9E		3	0.6	0.5

Table 3-12 QCS9075 G PMIC (PMM8650AU-0) SMPS regulator summary

Regulator	Circuit type	Irated (A)	Transient load step rating (A/100 ns)	Default booting voltage (V)
S1G_S2G_S3G_S4G	FTS527	24	2	0.824
S5G_S6G_S7G		18	2	0.824
S8G		6	2	-
S9G		6	2	-

Table 3-13 QCS8300 Primary PMIC (PMM8620AU-2), Secondary PMIC (PMM8650AU-0/PMM8620AU-0) LDO regulator summary

Regulator	Circuit type	I_{rated} (mA)	PMM8620AU (Primary PMIC) Default booting voltage (V)	PMM8650AU (Secondary PMIC) Default booting voltage (V)
L1	LDO515 LV NMOS 1200	1200	0.824	0.5
L2	LDO515 LV NMOS 1200	1200	0.824	0.9
L3	LDO515 LV NMOS 300	300	1.2	–
L4	LDO515 LV NMOS 1200	1200	0.88	1.2
L5	LDO515 LV NMOS 1200	1200	1.2	–
L6	LDO515 LV NMOS 1200	1200	0.912	1.8

Table 3-13 QCS8300 Primary PMIC (PMM8620AU-2), Secondary PMIC (PMM8650AU-0/PMM8620AU-0) LDO regulator summary (cont.)

Regulator	Circuit type	I_{rated} (mA)	PMM8620AU (Primary PMIC) Default booting voltage (V)	PMM8650AU (Secondary PMIC) Default booting voltage (V)
L7	LDO515 LV NMOS 300	300	0.88	1.8
L8	LDO515 MV PMOS 1200	1200	2.96	1.8
L9	LDO512 MV PMOS 150	150	3.072	1.8

Table 3-14 QCS9075 LDO regulator summary

Regulator	Circuit type	Irated (mA)	PMM8650AU-4 A PMIC Default booting voltage (V)	PMM8650AU-0 C PMIC Default booting voltage (V)	PMM8650AU-0 E PMIC Default booting voltage (V)	PMM8650AU-0 G PMIC Default booting voltage (V)
L1	LDO515 LV NMOS 1200	1200	0.824	1.2	–	–
L2	LDO515 LV NMOS 1200	1200	0.824	1.096	–	–
L3	LDO515 LV NMOS 300	300	0.752	1.2	–	–
L4	LDO515 LV NMOS 1200	1200	0.88	1.2	–	–
L5	LDO515 LV NMOS 1200	1200	0.88	1.2	–	–
L6	LDO515 LV NMOS 1200	1200	0.9	1.8	1.35	–
L7	LDO515 LV NMOS 300	300	0.88	1.8	–	–
L8	LDO515 MV PMOS 1200	1200	2.96	2.96	1.8	–
L9	LDO512 MV PMOS 150	150	3.072	1.8	–	–

3.4.1 FT-SMPS

FT-SMPS supports PWM and pulse-skipping modes. It also supports a retention mode, which is an ultra-low power state allowing significant efficient improvements in sleep mode. Following is a summary of key performance specifications for FTS527. Specifications are intended to apply over the temperature ranges defined in Operating conditions.

Table 3-15 FT-SMPS performance specifications

Parameter	Comments	Min	Typ	Max	Units
General characteristics					
Operating input voltage range (DC)	V_{IN} range for general compliance	3.1	–	3.5	V
Extended input voltage range (short duration transient)	<1 ms	3.0	–	3.6	V
Output voltage range	MV range	0.600	–	1.952	V
	LV range	0.300	–	1.372	V
Switching frequency	Supported Fs range	2.13	4.8	6.4	MHz

Table 3-15 FT-SMPS performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
NPM, any number of phases					
Rated steady-state load current per phase	LV range	–	–	6	A
	MV range (Vset > 1.8)	–	–	3	A
	MV range (Vset $\leq$ 1.8)	–	–	3.5	A
DC output voltage accuracy	VREG $\geq$ 0.8	-2	–	2	%
	VREG < 0.8	-16	–	16	mV
Ripple voltage	Unloaded through onset of PWM-CCM operation, 20 MHz BW limited Ripple measured across C_{OUT} where FB is tapped Guidance only since combined with transient for AC regulation window.	–	15	40	mVpp
Ground current					
Ground current referred to VDD_VSYS (NPM)	No load, 25°C Single phase				
	F_s = 3.2 MHz	–	0.100	0.125	mA
	F_s = 4.8 MHz	–	0.125	0.150	mA
	Multi-phase Current per phase				
	F_s = 3.2 MHz	–	0.120	0.145	mA
	F_s = 4.8 MHz	–	0.155	0.180	mA
Ground current Retention mode	No load, any number of phases	–	20	–	µA
NPM load transient, any number of phases					
Load transient dip/bump voltage disturbance	Any phase count 2 A load step per phase, transient slew ~100 ns	-40	–	70	mV
Load transient dip/bump voltage disturbance	Any phase count 1 A load step per phase, transient slew ~100 ns	-40	–	70	mV
Retention mode, any number of phases					
DC output accuracy, retention mode	DC error relative to programmed VSET Includes line and load regulation	-40	–	40	mV
Ripple voltage, retention mode	No load to max rated RM loading (DC) 20 MHz bandwidth limited. C_{OUT} = 2 × 15 µF or 2 × 22 µF or 4 × 10 µF	–	40	–	mVpp
Ripple voltage, retention mode	LV range; No load to max rated RM loading (DC) 20 MHz bandwidth limited. C_{OUT} = 1 × 22 µF or 2 × 10 µF, also MV configuration with 3 × 10 µF	–	50	–	mVpp
Ripple voltage, retention mode	MV range No load to max rated RM loading (DC) 20 MHz BW limited C_{OUT} = 1 × 22 µF or 2 × 10 µF	–	70	–	mVpp

Table 3-15 FT-SMPS performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Transition specifications					
Mode transition V_{OUT} disturbance	PWM to RM or RM to PWM; test condition is fixed load of 1 mA	-40	–	40	mV
Other general characteristics					
Enable warm-up time	Time from enable to start of V_{OUT} ramping single phase	–	15	–	µs
	Multiphase	–	35	–	µs
Enable (SS) or voltage change (VS) stepper overshoot	Relative to settled value, 38.4 mV/µs setting	–	–	40	mV
Soft start and voltage stepper slew rate	Actual voltage ramping slew rate (not counting warm-up time)	19.2	–	38.4	mV/µs
Peak output impedance	1 kHz to 1 MHz. Guidance only	–	40	–	mΩ
Discharge impedance, strong pull down	If enabled, will only engage when regulator is turned off	–	50	–	Ω
Discharge impedance, leak pull down	Can be active while the regulator is on or off	–	350	–	kΩ

3.4.2 Linear regulators

NOTE

- The specifications in the following table for LV NMOS and MV PMOS LDOs require that the external component and PCB routing parasitics be in compliance with the targeted values listed in the *Understanding Low-Dropout (LDO) Regulators Application Note* (80-VT310-125).
- All specifications are defined with 100 mV headroom for LV NMOS and 200 mV headroom for MV PMOS (3.3 V PMIC input maintained), and measured at C_{OUT}, onboard inside the module, unless stated otherwise (an example for the exception would be dropout voltage). To account for DC-R from C_{OUT} to the module BGA.
- All usage of LDOs outside of the design guidelines must be approved by QTI.

The headroom for subregulated LDOs is defined as VSET_BUCK - VSET_LDO. For specifications that have multiple contributors, like overall DC error and dropout voltage, see the diagrams in the *Understanding Low-Dropout (LDO) Regulators Application Note* (80-VT310-125).

Low dropout (LDO) linear regulator designs are implemented within the PMM8650AU/PMM8620AU:

- LDO512:
  - PMOS rated for 150 mA (P150) – one (L9)
- LDO515:
  - NMOS rated for 1200 mA (N1200) – five (L1, L2, L4, L5, L6)
  - NMOS rated for 300 mA (N300) – two (L3, L7)
  - PMOS rated for 1200 mA (P1200) – one (L8)

LDO performance specifications are presented in the following table.

Table 3-16 LDO515 regulator specifications

Parameter	Comments		Min	Typ	Max	Units	Note
Input voltage range	LVN (parent regulator Vset must not exceed 2.04 V)		0.32	–	2.2	V	
	MVP		2.5	–	5.5	V	
Output voltage range	LV NMOS (UL = 1.968 V in retention)		0.32	–	2.0	V	
	MV PMOS (programmable range 1.504-3.544)		1.8	–	3.3	V	
V_{OUT} step size			–	8	–	mV	
Normal power mode							
Rated load current	Maximum load current at which all specifications are met below headroom.	LVN1200 and MVP1200 LVN300	1200 300	–	–	mA	[a]
	LVN: HR = 100 mV			–	–		
	MVP: HR = 200 mV						
	Higher load current is possible at increased headroom						
Overall DC error (includes load and line regulation,temperature, VBAT, MBG variation, and trim error)	Measured at QAM BGA. $I_{RATIO} = I_{LOAD}/I_{RATED}$ LVN: HR = 100 mV MVP: HR = 200 mV Format: X + Y X = performance at LDO sense point Y = package + QAM PCB routing DCR contribution	LVN ($V_{OUT} \geq 0.65$ V)	- 2.0% - (Y mV) × I_{RATIO}		+2.0%	$\%V_{OUT}$	
		MVP	- 1.2% - (Y mV) ×IRATIO	–	+1.2%	$\%V_{OUT}$	
Load transient undershoot, overshoot – 1 µs ramp	Measured at C_{OUT}, compared to final settled value. $C_{OUT} = C_{nom}$. $I_{BASELINE} = 0.01 \times I_{RATED}$ or higher, Load step and headroom specified below, Ramp time = 1 µs						
	LVN1200, MVP1200: 600 mA step LVN300: 150 mA step	TE Disabled LVN	-40	–	+40	mV	[c]
	LVN: HR = 100 mV	TE Enabled LVN	-30	–	+20	mV	[c] [d]

Table 3-16 LDO515 regulator specifications (cont.)

Parameter	Comments		Min	Typ	Max	Units	Note
	MVP: HR = 200 mV	MVP	-40	–	40		
Startup settling time	From start of ramp to within 1% of final value with no load. UL is with maximum C_{OUT}, max V_{set}. LL is with min C_{OUT}, min V_{set}. LVN startup time depends on V_{set} and Stepper rate setting.	LVN	8	–	500	µs	e
		MVP	10	–	300		
Startup in-rush current	Averaged over 1 µs window, with no load. Variation due to bulk cap size	LVN1200	–	150	650	mA	
		MVP1200	–	300	500		
		LVN300	–	50	650		
Dropout voltage	LVN. From parent buck C_{OUT} to LDO sense point. Load at I_{RATED}		–	–	54	mV	f
	MVP. From parent buck C_{OUT} to LDO sense point. Load at I_{RATED}		–	–	150	mV	
Overcurrent protection detection threshold (I_{OCP})	Threshold for OCP detection. OCP interrupt and self-shutdown are based on tripping this threshold. LVN: HR = 100 mV MVP: HR = 200 mV	LVN1200	2400	–	4000	mA	
		MVP1200	2400	–	3600		
		LVN300	600	–	900		
Output noise density	Measured at C_{OUT}. LDO contribution only, assumes clean V_{IN}.	LVN: HR = 100 mV				µV/√Hz	
		1 kHz ≤ f ≤ 10 kHz	–	3	–		
		10kHz ≤ f ≤ 100kHz	–	1.5	–		
		100 Hz ≤ f ≤ 1 kHz	–	1.2	–		
		100 kHz ≤ f ≤ 1 MHz	–	0.5	–		
		MVP: HR = 200 mV					
		100 Hz ≤ f ≤ 1 kHz	–	1.5	–		
		1 kHz ≤ f ≤ 10 kHz	–	0.75	–		
		10kHz ≤ f ≤ 100 kHz	–	0.5	–		
		100 kHz ≤f≤1MHz	–	0.25	–		
Ground current, no load	Measured at the battery. MVO I_Q may be much higher if LDO is operated in drop-out condition.	LVN	–	110	200	µA	
		MVP	–	32	40		

Table 3-16 LDO515 regulator specifications (cont.)

Parameter	Comments		Min	Typ	Max	Units	Note
Ground current, with load	In addition to no load ground current. % of the load current MVP I_{GND}/I_{LOAD} ratio varies over load current range	LVN	–	–	0.5	$\%I_{LOAD}$	
		MVP (for I_{LOAD} > 10 mA in NPM)	–	0.5	2.5		
LDO discharge time to below 100 mV	Strong pull down enabled. Typical at nominal C_{OUT}, UL is with maximum C_{OUT}.	LVN	–	0.1	2	ms	
		MVP	–	0.4	4		
VREG_OK threshold – during enable or step up	LVN		85%	90%	95%	V_{OUT}	
	MVP		V_{SET}-280 mV	V_{SET} -210 mV	V_{SET} -140 mV		
Forced bypass mode							
Ground current	LVN		–	2	5	μA	[g]
	MVP		–	0.5	1		

[a] The rated current is the current at which the regulator meets all specifications. Higher currents can be allowed, but the regulator may need more headroom, (this is, the difference between $V_{IN}$and V_{OUT}). For low-power mode, the LDO should be switched to normal power mode if the load current is expected to be above the rated current.

[b] Y = (package + QAM PCB routing DCR) * $I_{RATED}$for each regulator output.

[c] TE is transient enhancer, and is a feature available for LVN LDOs, and is enabled by default.

[d] At high temperature and some process corners, the pass device leakage causes the output voltage to float up under no-load conditions. The leakage pull down may need to be enabled to meet the specifications.

[e] The settling time is for startup, and any upward voltage change with the rated load capacitance. Time is increased with larger load capacitance. Settling time of a downward voltage change depends on the load current.

[f] Dropout voltage is defined as follows:

- Apply the specified load current.
- Set V_{IN}= V_{OUT}+ 0.5 V.
- Measure the output voltage.
- Reduce V_{IN}until $V_{OUT}$is reduced by 100 mV.
- Calculate dropout voltage as V_{IN}- V_{OUT}in this condition.

[g] In bypass mode, there is an active gate to source clamp to protect the LV NMOS.

Table 3-17 LDO512 regulator specifications

Parameter	Comments	Min	Typ	Max	Units	Note
Input voltage range	NMOS	0.32	–	1.4	V	
	LV PMOS (parent regulator Vset must not exceed 2.04 V)	1.8	–	2.2		
	MV PMOS	2.5	–	5.5		

Table 3-17 LDO512 regulator specifications (cont.)

Parameter	Comments		Min	Typ	Max	Units	Note
Output voltage range	MV PMOS		1.504	–	3.544	V	
V_{OUT} step size			–	8	–	mV	
Normal power mode							
Rated load current	Maximum load current at which all specifications are met below headroom. MV PMOS: HR = 500 mV Higher load current is possible at increased headroom	MV PMOS	150	–	–	mA	[a]
Overall DC error (includes load and line regulation, temperature, Vbatt, MBG variation, and trim error)	Measured at QAM BGA. $I_{RATIO} = I_{LOAD}/I_{RATED}$ MV PMOS: HR = 500 mV Format: X + Y + Z X = performance at LDO sense point Y= On-die routing DCR contribution Z= PCB routing DCR contribution	MV PMOS	- 2% - (6 mV + 15 mV) × I_{RATIO}	–	+2%	%V_{OUT}	[b] [c]
Load transient undershoot, overshoot	Max load step of 0.5 × I_{RATED} in 1 µs, with baseline current of 0.01 × I_{RATED} or higher. Compared to final settled value. MV PMOS: HR = 500 mV	MV PMOS	-50	–	70	mV	
Startup settling time	To within 1% of final value. UL is with maximum C_{OUT}.NMOS startup time depends on VSET and stepper rate setting	MV PMOS (V_{OUT} = 3.3 V)	–	–	600	µs	[d]
Startup in-rush current	During start-up. Variation due to bulk capacitor size.	MV PMOS	–	25	300	mA	
Dropout voltage	MV PMOS. From parent buck C_{OUT} to LDO sense point. Load at I_{RATED}		–	–	300	mV	[e]
Over current protection detection threshold (IOCP)	Threshold for OCP detection. OCP interrupt and self-shutdown are based on tripping this threshold.	MV PMOS	200	–	550	mA	

Table 3-17 LDO512 regulator specifications (cont.)

Parameter	Comments		Min	Typ	Max	Units	Note
Output noise density	Measured at C_{OUT}. LDO contribution only, assumes clean V_{IN}.	MV PMOS: HR = 500 mV				µV/√Hz	
		100 Hz ≤ f ≤ 1 kHz	–	11	–		
		1 kHz ≤ f ≤ 10 kHz	–	3.5	–		
		10 kHz ≤ f ≤ 100 kHz	–	1.2	–		
		100 kHz ≤ f ≤ 1 MHz	–	0.7	–		
Ground current, no load	Measured at the battery. IQ may be much higher if LDO is operated in drop-out condition.	MV PMOS	–	85	120	µA	
Normal mode							
Ground current, with load	% of the load current	MV PMOS	–	0.4	0.8	% I_{LOAD}	
LDO discharge time to below 100 mV	Strong pull down enabled. Typical at nominal C_{OUT}, UL is with maximum C_{OUT}.	MV PMOS	–	–	2	ms	
VREG_OK threshold – during enable or step up			85%	90%	95%	V_{OUT}	
Forced bypass mode							
Ground current		MV PMOS	–	0.5	1	µA	

[a] The rated current is the current at which the regulator meets all specifications. Higher currents can be allowed, but the regulator may need more headroom, (this is, the difference between V_{IN} and V_{OUT}). For low-power mode, the LDO should be switched to normal power mode if the load current is expected to be above the rated current.

[b] At high temperature and some process corners, the pass device leakage causes the output voltage to float up under no-load conditions. The leakage pull down may must be enabled to meet the specifications.

[c] Y = (package + QAM PCB routing DCR) × $I_{RATED}$for each regulator output.

[d] The settling time is for startup, and any upward voltage change with the rated load capacitance. Time is increased with larger load capacitance. Settling time of a downward voltage change depends on the load current.

[e] Dropout voltage is defined as follows:

- Apply the specified load current.
- Set V_{IN}= V_{OUT}+ 0.5 V.
- Measure the output voltage.
- Reduce V_{IN}until $V_{OUT}$is reduced by 100 mV.
- Calculate dropout voltage as V_{IN}- V_{OUT}in this condition.

3.5 Power-on sequence

Table 3-18 PMM8620AU/PMM8650AU power-on sequence for QCS8300

QCS8300
VSYS (VREG_PMIC_IN_3P3): 3.3 V input voltage supply to primary PMIC (PMM8620AU) and secondary PMIC (PMM8650AU)
PM_KPD_PWR_N (pin E13, PWR_EN_N) of primary PMIC (PMM8620AU) and secondary PMIC (PMM8650AU)
VREG_1P8_SYS_A
PMICA_GPIO3
PMICA_GPIO5
S9C
S5A
S6A
L1A
S1C
S7A_S8A
L2A
S2C_S3C
PMICA_GPIO7
L9C
SLEEP_CLK of primary PMIC (PMM8620AU)
L3A
L8C
S5C
L2C
L1C
L5A
L4A
L7A
L7C
L9A
L8A
L4C
S6C_S7C_S8C
S9A_S1A
S2A_S3A_S4A
S4C
L6A
PMICA_GPIO2
LNBB_CLK1 of primary PMIC (PMM8620AU)

Table 3-18 PMM8620AU/PMM8650AU power-on sequence for QCS8300 (cont.)

QCS8300
LNBB_CLK2 of primary PMIC (PMM8620AU)
LNBB_CLK3 of primary PMIC (PMM8620AU)
PMICA_GPI011
PON_RESET_N of primary PMIC (PMM8620AU)
PS_HOLD of primary PMIC (PMM8620AU)

Table 3-19 PMM8620AU/PMM8650AU power-on sequence for QCS8275

QCS8275
VSYS (VREG_PMIC_IN_3P3): 3.3 V input voltage supply to primary PMIC (PMM8620AU) and secondary PMIC (PMM8650AU)
PM_KPD_PWR_N (pin E13, PWR_EN_N) of primary PMIC (PMM8620AU) and secondary PMIC (PMM8650AU)
VREG_1P8_SYS_A
PMICA_GPIO3
S9A
S5A
S6A
L1A
S1C
S7A_S8A
L2A
S2C_S3C
S4A
L9C
SLEEP_CLK of primary PMIC (PMM8620AU)
L3A
L8C
S5C
L2C
L1C
L5A
L4A
L7A
L7C
L9A
L8A
L4C
S6C_S7C_S8C
S9C
S1A

Table 3-19 PMM8620AU/PMM8650AU power-on sequence for QCS8275 (cont.)

QCS8275
S2A
S4C
L6A
PMICA_GPIO2
LNBB_CLK1 of primary PMIC (PMM8620AU)
LNBB_CLK2 of primary PMIC (PMM8620AU)
PMICA_GPIO11
PON_RESET_N of primary PMIC (PMM8620AU)
PS_HOLD of primary PMIC (PMM8620AU)

Table 3-20 Power-on sequence for QCS9075

VSYS (VREG_PMIC_IN_3P3): 3.3 V input voltage supply to PMICs
KPD_PWR_N (pin E13, PWR_EN_N) to all PMICs
VREG_1P8_SYS_A
GPIO_03A
GPIO_05A
S4E
S9A
S1C_2C
S5E_6E
L1A
S8E
S1A_2A_3A
L2A
S3C_4C
S4A
VREF_IX_A
SLEEP_CLK
L3C
L8E
S7E
L6A
S9E
L1C
L4A
L7A
L6C
L9A

Table 3-20 Power-on sequence for QCS9075 (cont.)

L8A
L4C
S1E_2E_3E
S5G_6G_7G
S6C_7C_8C_9C
S6A_7A_8A
S1G_2G_3G_4G
L5A
L5C
L9C
L9C
GPIO_02A
LNBB_CLK1
LNBB_CLK2
LNBB_CLK3
GPIO_11A
PON_RESET_N

3.6 VDD_VSYS undervoltage and overvoltage lockout

In order to stay ON, VDD_VSYS must remain between the UVLO threshold and the OVLO threshold. If these thresholds are exceeded, a fault will occur and the IC will shut down. UVLO/OVLO-related voltage specifications are listed in the following table.

Table 3-21 UVLO and OVLO thresholds (PMM8650AU/PMM8620AU)

Parameter	Nominal	Units
Undervoltage threshold	2.75	V
Over voltage threshold [a]	3.85	V

[a] Monitor enabled during power on.

3.7 Option hardwired controls

Table 3-22 QCS9075 PMICs PON option pin table

PMIC Pin	A PMIC	C PMIC	E PMIC	G PMIC
GPIO_01	Free use	GND	Float	GND
GPIO_02	Free use	GND	GND	Float
GPIO_03	UFS0 Float: L8A = 2.5 V (UFS3.x) 10 kΩ to GND: L8A = 2.96 V (UFS2.x)	UFS1 Float: L8C = 2.5 V (UFS3.x) 10 kΩ to GND: L8C = 2.96 V (UFS2.x)	Free use	Free use

3.8 General housekeeping

The PMIC includes many circuits that support housekeeping functions – various tasks that must be performed to keep the device in order. Integration of these functions reduces the external parts count and the associated size and cost. Housekeeping functions include an analog switch matrix, multiplexers, and voltage scaling; an HK/XO ADC circuit; system clock circuits; a real-time clock for time and alarm functions; and overtemperature protection.

3.8.1 38.4 MHz XO circuits

An external crystal and thermistor network are supplemented by on-chip circuits to generate the desired 38.4 MHz reference signal. The 38.4 MHz XO circuits initialize and maintain valid pulse waveforms, and measure time intervals for higher-level handset functions. Multiple controllers manage the XO warm-up and signal buffering, and generate the desired clock outputs (all derived from one source):

- Low-noise BB clock outputs: LNBB_CLK1, LNBB_CLK2, LNBB_CLK3

The XTAL_IN and XTAL_OUT pins are incapable of driving a load – the oscillator will be significantly disrupted if either pin is externally loaded.

The 38.4 MHz XO circuit and related performance specifications are listed in the following tables.

Table 3-23 LNBB_CLKx specifications

Parameter	Test condition or Comment	LLimit	Typ	ULimit	Unit
Frequency	QCS8300, QCS8275, QCS9075		19.2		MHz
Duty cycle		48	50	52	%
Output voltage swing			1.2		V
Phase noise	@ 10 Hz		-86		dBc/Hz
	@ 100 Hz		-110		dBc/Hz
	@ 1 kHz		-136		dBc/Hz
	@ 10 kHz		-144		dBc/Hz
	@ 100 kHz		-144		dBc/Hz
	@ 1 MHz		-144		dBc/Hz

3.8.2 38.4 MHz XO crystal requirements

Guidance is available within the*38.4 MHz Modem Crystal For Industrial Temperature And Automotive (Aec-Q200) Qualification Requirements And Approved Suppliers* (80-NJ458-29) document. This document includes:

- Data needed from crystal suppliers to demonstrate compliance
- Approved suppliers for different crystal configurations
- Description of various schematic options

3.8.3 Sleep clock

The sleep clock (32.7645 kHz) is generated in one of the following ways:

- Using the calibrated low-frequency RC oscillator
  - Periodically using the 38.4 MHz XO signal for calibration, achieving accuracy suitable for the real-time clock
- Using the XO/HFRC circuit and dividing its output to create a 32.7645 kHz signal

Table 3-24 Sleep buffer specifications

	Min	Typ	Max	Unit
Clock frequency		32.7645		kHz
Output voltage swing		1.8		V
Duty cycle (after PSI load)	45		55	%

3.8.4 Real-time clock

Table 3-25 RTC performance specifications

Parameter	Min	Typ	Max	Unit	Notes
RTC accuracy (XO is RTC source)	-100		100	ppm	Mission mode/STR
RTC accuracy (XO off, CalRC is RTC source)	-7000		7000	ppm	Deep sleep/off mode

NOTE In addition to accumulated error based on RTC accuracy, a power-cycle can introduce an error of up to 1 s.

3.8.5 Analog multiplexer and scaling circuits

A set of analog switches, analog multiplexers, and voltage-scaling circuits select and condition a single analog signal for routing to the on-chip HK/XO ADC. The multiplexer and scaling functions are summarized in the following table.

Table 3-26 Analog multiplexer and scaling circuits

Ch. number (hexadecimal)	Description	Source	Scaling	Internal pull-up	Input voltage (V)
0	OFFSET_REF	REF_GND	1/1	Open	0 to 1.875
1	1P25VREF	Internal: MBG	1/1	Open	0 to 1.875
2	VREF_VADC	Internal: VADC LDO	1/1	Open	0 to 1.875
3	DIE_TEMP	Internal: TEMP_ALARM	1/1	Open	0 to 1.875
4	AMUX_THM1	AMUX_1	1/1	Open	0 to 1.875
5	AMUX_THM2	AMUX_2	1/1	Open	0 to 1.875
6	AMUX_THM3	AMUX_3	1/1	Open	0 to 1.875
7	AMUX_THM4	AMUX_4	1/1	Open	0 to 1.875
8	AMUX_THM5	AMUX_5	1/1	Open	0 to 1.875
9	AMUX_THM6	AMUX_6	1/1	Open	0 to 1.875
A	AMUX1_GPIO	GPIO_09 MV	1/1	Open	0 to 1.875
B	AMUX2_GPIO	GPIO_10 MV	1/1	Open	0 to 1.875
C	AMUX3_GPIO	GPIO_11 MV	1/1	Open	0 to 1.875
D	AMUX4_GPIO	GPIO_12 MV	1/1	Open	0 to 1.875
44	AMUX_THM1	AMUX_1	1/1	100K	0 to 1.875
45	AMUX_THM2	AMUX_2	1/1	100K	0 to 1.875
46	AMUX_THM3	AMUX_3	1/1	100K	0 to 1.875
47	AMUX_THM4	AMUX_4	1/1	100K	0 to 1.875

Table 3-26 Analog multiplexer and scaling circuits (cont.)

Ch. number (hexadecimal)	Description	Source	Scaling	Internal pull-up	Input voltage (V)
48	AMUX_THM5	AMUX_5	1/1	100K	0 to 1.875
49	AMUX_THM6	AMUX_6	1/1	100K	0 to 1.875
4A	AMUX1_GPIO	GPIO_09 MV	1/1	100K	0 to 1.875
4B	AMUX2_GPIO	GPIO_10MV	1/1	100K	0 to 1.875
4C	AMUX3_GPIO	GPIO_11 MV	1/1	100K	0 to 1.875
4D	AMUX4_GPIO	GPIO_12 MV	1/1	100K	0 to 1.875
8A	AMUX1_GPIO	GPIO_09 MV	1/3	Open	0 to 3.3
8B	AMUX2_GPIO	GPIO_10 MV	1/3	Open	0 to 3.3
8C	AMUX3_GPIO	GPIO_11 MV	1/3	Open	0 to 3.3
8D	AMUX4_GPIO	GPIO_12 MV	1/3	Open	0 to 3.3
8E	VPH_PWR	VPH_PWR	1/3	Open	0 to 3.3
FF	Off		N/A	N/A	N/A

3.8.6 ADC

The ADC electrical specifications for the temperature range of -40ºC to 85ºC are summarized in the following tables.

Table 3-27 Non-PRTSS ADC electrical specifications

Specification	Test condition	Min	Typ	Max	Units
1/1 channel end-to-end gain error for absolute calibration	Input = 0.0 V to 1.8 V	-1.5	–	1.5	%
1/1 channel end-to-end offset error for absolute calibration	Input = 0.0 V to 1.8 V	-2	±0.5	2	mV
1/1 channel end-to-end accuracy with internal pull-up and ratiometric calibration	Ratiometric calibration data result for ratio (reported ratio will be within specified tolerance of actual ratio, where ratio error % = measured ratio % -actual ratio %)	-0.6	0.3	0.6	%
1/3 channel end-to-end accuracy	Input = 0.5 V to 5.25 V	-1.5	–	1.5	%
ADC resolution (LSB) for absolute measurement	1/1 channel 1/3 channel For 1/1 channel: 16 bit signed from 0 V (0x0000) to 2.0196 V (0x7999) For 1/3 channel: 16 bit signed from 0 V (0x0000) to 6.0588 V (0x7999)	–	64.879 194.637	–	μV μV
ADC resolution (LSB) for ratio measurement	1/1 channel For 1/1 channel: 14 bit ratio from 0% (0x0000) to 100% (0x4000)	–	0.006104	–	%
ADC LDO voltage		1.828	1.875	1.922	V
ADC sample clock		–	4.8	–	MHz
ADC conversion time	1K decimation ratio, 4.8 MHz sample clock, SINC2 conversion, no clock dithering	–	654	700	μs
Current consumption – ADC only	VADC active – does not include other PMIC infrastructure	–	450	500	μA

Table 3-27 Non-PRTSS ADC electrical specifications (cont.)

Specification	Test condition	Min	Typ	Max	Units
Current consumption – ADC and required infrastructure hardware	VADC, MBG, and ADC clock source active	–	1000	1500	µA
100K pull-up	Trimmed value	99.5	100	100.5	KΩ
Pull-up temperature coefficient		-150	–	150	ppm/ºC
Pull-up aging	Value change over time and temperature cycling	-0.5	–	0.5	%
1/1 channel AMUX input resistance		10	–	–	MΩ
1/3 channel AMUX input resistance		1	–	–	MΩ
Leakage current – all pins using internal pull-up resistors	With VBATT and aVdd present, apply 1.8 V to pin and monitor current	–	–	10	nA

Table 3-28 PRTSS ADC electrical specifications

Specification	Test Condition	Min	Typ	Max	Units
1/1 channel end-to-end gain error for absolute calibration	Input = 0.0 V to 1.8 V	-1.5	–	1.5	%
1/1 channel end-to-end offset error for absolute calibration	Input = 0.0 V to 1.8 V	-2	±0.5	2	mV
1/3 channel end-to-end accuracy	Calibrated data result; input = 0.5 V to 5.25 V	-2.0	–	2.0	%
ADC resolution (LSB) for absolute measurement	1/1 channel, absolute calibration	–	64.879	–	µV
ADC LDO voltage		1.828	1.875	1.922	V
ADC sample clock		–	4.8	–	MHz
ADC conversion time	1K decimation ratio, 4.8 MHz sample clock, SINC2 conversion, no clock dithering	–	654	700	µs
Current consumption – ADC only	VADC active – does not include other PMIC infrastructure	–	450	500	µA
Current consumption – ADC and required infrastructure hardware	VADC, MBG, and ADC clock source active	–	1000	1500	µA
1/1 channel AMUX input resistance		10	–	–	MΩ
1/3 channel AMUX input resistance		1	–	3	MΩ
Leakage Current – All pins using internal pull-up resistors	With VBATT and aVdd present, apply 1.8 V to pin and monitor current, -40ºC to 85ºC, VBATT = 2.5 V to 5.25 V	–	–	10	nA

3.9 GPIO specifications

The 12 GPIO ports are digital I/Os that can be programmed for a variety of configurations. The digital I/O logic thresholds are listed in Table 3-30 to Table 3-34.

NOTE All unused GPIO pins, except for the following, should be configured as digital inputs with 10 µA pull-down (their default state).

Table 3-29 Programmable GPIO configurations

Configuration type	Configuration description
Input	▪ No pull-up ▪ Pull-up (1.5 µA, 30 µA, or 31.5 µA) ▪ Pull-down (10 µA) ▪ Keeper
Output	▪ Open-drain or CMOS ▪ Inverted or noninverted ▪ Programmable drive current

NOTE GPIOs 9 to 12 can be MUXed to the ADC for analog measurements.

Table 3-30 GPIO_MV digital I/O characteristics

Parameter		Comments [a]	Min	Typ	Max	Units
V_{IH}	High-level input voltage	–	0.65 × V_{IO}	–	–	V
V_{IL}	Low-level input voltage	–	–	–	0.35 × V_{IO}	V
V_{SHYS}	Schmitt hysteresis voltage	–	0.1 × V_{IO}	–	–	mV
I_L	Input leakage current [b]	–	-0.20	–	+0.20	µA
V_{OH}	High-level output voltage	–	0.8 × V_{IO}	–	V_{IO}	V
V_{OL}	Low-level output voltage	–	0	–	0.2 × V_{IO}	V

[a] VIO is the supply voltage for the SoC/PMIC interface (most PMIC digital I/Os).

[b] GPIO pins comply with the input leakage specification only when configured as a digital input or set to the tri-state mode.

Table 3-31 GPIO_MV VOL and VOH and minimum load current

Supply voltage	V_{OL}, V_{OH}	Minimum load current		
		Low strength driver	Medium strength driver	High strength driver
1.8 V	V_{OH} = 0.8 × V_{IO}	0.15 mA	0.3 mA	0.6 mA
	V_{OL} = 0.2 × V_{IO}			
3.6 V	V_{OH} = 0.8 × V_{IO}	0.25 mA	0.5 mA	1 mA
	V_{OL} = 0.2 × V_{IO}			

Table 3-32 GPIO_LV digital I/O characteristics

Parameter		Comments [a]	Min	Typ	Max	Units
V_{IH}	High-level input voltage	–	0.9	–	–	V
V_{IL}	Low-level input voltage	–	–	–	0.6	V

Table 3-32 GPIO_LV digital I/O characteristics (cont.)

Parameter		Comments [a]	Min	Typ	Max	Units
V_{SHYS}	Schmitt hysteresis voltage	–	180	–	–	mV
I_L	Input leakage current [b]	–	-0.20	–	+0.20	µA
V_{OH}	High-level output voltage	–	0.8 × V_{IO}	–	V_{IO}	V
V_{OL}	Low-level output voltage	–	0	–	0.2 × V_{IO}	V

[a] VIO is the supply voltage for the SoC/PMIC interface (most PMIC digital I/Os).
[b] GPIO pins comply with the input leakage specification only when configured as a digital input or set to the tri-state mode.

Table 3-33 GPIO_LV VOL and VOH and minimum load current

Supply voltage	V_{OL}, V_{OH}	Minimum load current		
		Low strength driver	Medium strength driver	High strength driver
1.8 V	V_{OH} = 0.8 × V_{IO}	1 mA	1.5 mA	2 mA
	V_{OL} = 0.2 × V_{IO}			

Table 3-34 Digital I/O characteristics (PS_HOLD)

Parameter		Comments [a]	Min	Typ	Max	Units
Digital input	V_{IH}	V_{IO} = 1.8 V	1.2	–	–	V
	V_{IL}		–	–	0.6	V
	$V_{HYSTERESIS}$		184	–	–	mV

[a] V_{IO} is the supply voltage for the SoC/PMIC interface (most PMIC digital I/Os).

4 Mechanical information

4.1 Device physical dimensions

The PMM8650AU/PMM8620AU is available in the 181 MSP that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 181 MSP has a 9.3 mm by 9.3 mm body, with a maximum height of 1.18 mm. Pin 1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 181 MSP outline drawing is shown in Figure 4-1.

NOTE Click the following link to download the *Package Outline Drawing, MSP181, 9.3 x 9.3x 1.18 mm, S266, M750* (NT90-23629-1) from the Qualcomm website.

https://docs.qualcomm.com/bundle/NT90-23629-1/resource/NT90-23629-1.pdf

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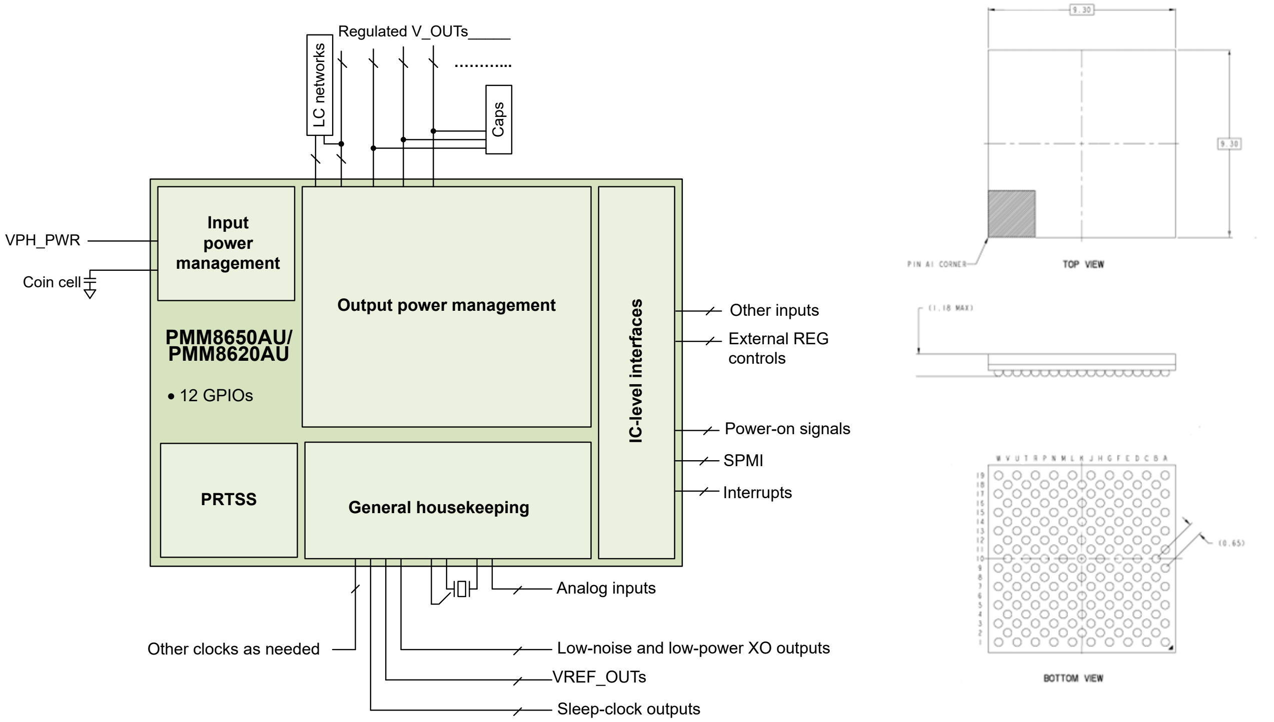


Figure 4-1 181 MSP outline drawing

NOTE This is a simplified outline drawing. Click the link on the previous page to download the complete, up-to-date package outline drawing.

4.2 Part marking

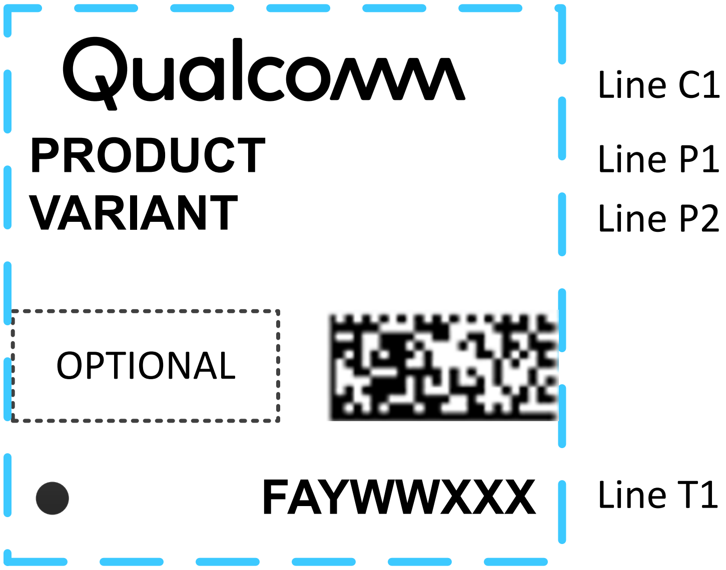


Figure 4-2 Device marking (top view, not to scale)

Table 4-1 Device marking line definitions

Line	Marking	Description
C1	QUALCOMM	Qualcomm logo
P1	PRODUCT	Qualcomm Technologies, Inc. (QTI) product name ■ PMM8650AU ■ PMM8620AU
P2	VARIANT	Device variant information ■ See Table 4-3 for the assigned values.
	Blank or random	■ Optional/additional trace information ■ Device specific 2D bar code
T1	● FAYWWXXX	Pin 1 indicator F = wafer fab source of supply code ■ F = F for TSMC A = assembly (ball drop) code ■ A = E for ASE, Taiwan ■ A = K for SPIL, Taiwan Y = single/last digit of year WW = two-digit work week of year specified by Y XXX = traceability number

4.3 Device ordering information

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code shown in Table 4-2 and Table 4-3.

Table 4-2 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [a]
Symbol definition	**Product name**	**Configuration code**	**Package type**	**Number of pins**	**Package variable**	**Additional package information**	**Shipping package**	**Product revision**	**Source code**	**Feature code**
Example 1	PMM-8620AU	-2	-MSP	181			-TR	-02	-0	-00
Example 2	PMM-8620AU	-0	-MSP	181			-TR	-02	-0	-05

[a] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

- Primary PMIC Example: PMM-8620AU-2-MSP181-TR-02-0-00
- Secondary PMIC Example: PMM-8620AU-0-MSP181-TR-02-0-05

NOTE The shipping package is either TR (tape and reel) or MT (matrix tray).

Table 4-2 shows the current package-type nomenclature. For legacy parts, the Oracle short description has the position of package type and number of pins reversed.

Device identification details for all samples available to date are summarized in Table 4-3.

Table 4-3 QCS8300, QCS8275 PMIC device identification details

Device	Sample type	Product configuration code (P)	Product revision code (RR)	Feature code (BB) [a]	Hardware version	Source configuration code (S) [b]
PMM8620AU	ES1	2	02	00	v2.0	0
PMM8620AU	ES2	2	02	01	v2.0	0
PMM8620AU	CS CS date code are as follows: ASE: 437 SPIL: 437	2	02	01	v2.0	0
PMM8620AU	ES1	0	02	05	v2.0	0
PMM8620AU	CS [c] CS date code are as follows: ASE: 437 SPIL: 437	0	02	05	v2.0	0

[a] BB is the feature code that identifies an IC’s specific feature set, which distinguishes it from other versions or variants.

[b] S is the source configuration code that identifies all the qualified die fabrication-source combinations available when the particular sample type was shipped. S values are defined in Table 4-5.

[c] All devices with YWW ≥ 437 date code or later are CS quality. However, devices with earlier date codes may also be CS quality. Contact your customer service representative for CS part marking with date codes prior to YWW ≥ 437.

Table 4-4 QCS9075 PMIC device identification details

Device	Sample type	Product configuration code (P)	Product revision code (RR)	Feature code (BB) [a]	Hardware version	Source configuration code (S) [b]
PMM8650AU	ES1	4	02	09	v2.0	0
PMM8650AU	CS [c] CS date code are as follows: ASE: 434 SPIL: 434	4	02	09	v2.0	0
PMM8650AU	ES1	0	02	04	v2.0	0
PMM8650AU	CS [d] CS date code are as follows: ASE: 402 SPIL: 402	0	02	04	v2.0	0

[a] BB is the feature code that identifies an IC’s specific feature set, which distinguishes it from other versions or variants.

[b] S is the source configuration code that identifies all the qualified die fabrication-source combinations available when the particular sample type was shipped. S values are defined in Table 4-5.

[c] All devices with YWW ≥ 434 date code or later are CS quality. However, devices with earlier date codes may also be CS quality. Contact your customer service representative for CS part marking with date codes prior to YWW ≥ 434.

[d] All devices with YWW ≥ 402 date code or later are CS quality. However, devices with earlier date codes may also be CS quality. Contact your customer service representative for CS part marking with date codes prior to YWW ≥ 402.

Table 4-5 Source configuration code

S value	F value = F	A value = E	A value = K
0	TSMC	ASE, Taiwan	SPIL, Taiwan

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-6.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **PMM8650AU/PMM8620AU rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The PMM8650AU/PMM8620AU devices are classified as MSL3; the qualification temperature was 260°C +0°/-5°C.*** This qualification temperature (260°C +0°/-5°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the Qualcomm website. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click the following link to download the *PMM865XAU Package Thermal Model Icepak and Flotherm* from the Qualcomm website.

https://docs.qualcomm.com/bundle/HS11-31752-5HW/resource/HS11-31752-5HW.zip

NOTE After successfully logging in, the document is downloaded. Make this document a favorite to be notified of any changes.

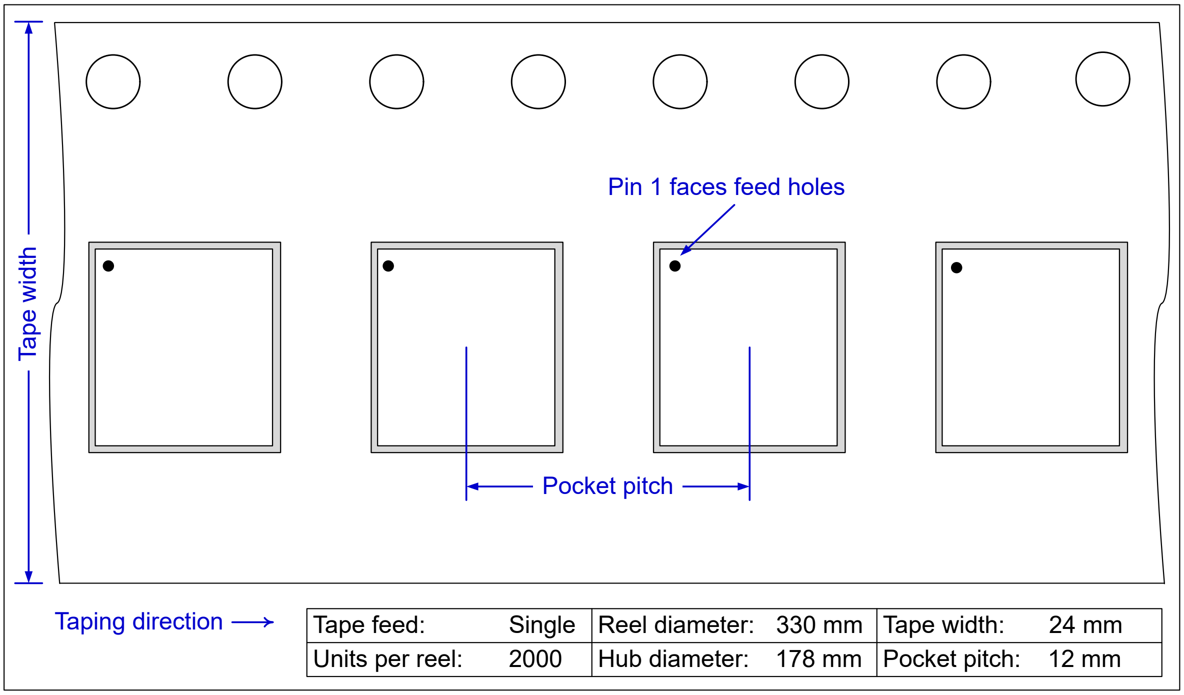
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI carrier tape systems conform to EIA-481 standards.

A simplified sketch of the PMM8650AU/PMM8620AU tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	12 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

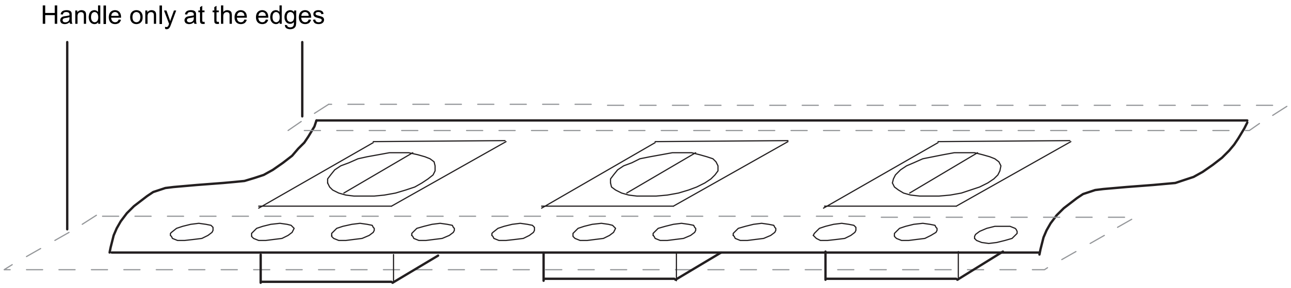


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

PMM8650AU/PMM8620AU devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. See the *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Device moisture sensitivity level.

5.3 Handling

Tape handling was described in Tape and reel information. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

Wafer-level packages such as the MSP181 should not be baked.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC405 composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the Qualcomm website.

https://docs.qualcomm.com/bundle/SM80-P0982-1/resource/SM80-P0982-1.pdf

NOTE After successfully logging in, the document is downloaded.

7 Part reliability

7.1 Reliability evaluation summary

PMM8650AU reliability evaluation report/plan for 9.3 × 9.3 × 1.18 mm 181 FC-BGA device, foundry source TSMC F6

Table 7-1 Silicon reliability results

Stress	ABV	Test#	Test method	Test conditions/Pre and Post ATE (Identify Temperature, RH, and Bias)	Requirements		Results	Comments
					S.S. per lot	# Lots	Fails/Total S.S.	
Test Group A – Accelerated Environment Stress Tests								
Preconditioning	**PC**	A1	JEDEC-J-STD-020, JESD22-A113	MSL 3, 3X reflow (Pre and Post ATE @ R & H)	231	12	0/2772	
Preconditioning + Biased HAST	**HAST**	A2	JEDEC-JESD22-A110	130°C/85%RH for 96 hours (Pre and Post ATE @ R & H)	77	6	0/462	
Preconditioning + Unbiased HAST/Temperature Humidity	**TH**	A3	JEDEC-JESD22-A101	85°C/85%RH for 1000 hours (Pre and Post ATE @ R)	77	6	0/462	
Preconditioning + Temperature Cycle	**TC**	A4	JEDEC-JESD22-A104	Ta=-55°C to +125°C for 1000 cycles (Pre and Post ATE @ R & H)	77	6	0/462	
High temperature storage life	**HTSL**	A6	JEDEC-JESD22-A103	Ta=+150°C for 500 hours (Pre and Post ATE @ R & H)	45	6	0/270	
Test Group B – Accelerated Lifetime Simulation Tests								
High temperature operating life	**HTOL**	B1	JEDEC-JESD22-A108	Tj=125°C for 1000 hours (Pre and Post ATE @ R, C & H)	77	3	0/231	

Table 7-1 Silicon reliability results (cont.)

Stress	ABV	Test#	Test method	Test conditions/Pre and Post ATE (Identify Temperature, RH, and Bias)	Requirements		Results	Comments
					S.S. per lot	# Lots	Fails/Total S.S.	
Early life failure rate	**ELFR**	B2	JESD22-A108	Tj=125°C for 48 hours (Pre and Post ATE @ R & H)	800	3	1F/2400	1 unit failed for FTS_Sx_PWM_NLI RT/HT in ATE. PFA found Silicon and Nitrogen FEOL process defect between GOX and Poly of NMOSCAP. Enable T0 HVS screen with FT TP rev56. T48 BI will screen this failure mode and validate T0 HVS screen as a containment.
NVM endurance, data retention, and operational life	**EDR**	B3						Not applicable, no NVM memory on device
Test Group C – Package Assembly Integrity Tests								
Wire bond shear	**WBS**	C1						Not applicable, not a wirebonded package
Wire bond pull strength	**WBPS**	C2						Not applicable, not a wirebonded package
Solderability	**SD**	C3						Not applicable, not a leadframe package
Physical dimensions	**PD**	C4	JESD22-B100	Package Outline Drawing	10	6	0/60	CPK≥1.67
Solder ball shear	**SBS**	C5	JESD22-B117	5 balls each from a min. of 10 devices, ≥ 300 g/ball for pad opening 350 µm	10	6	0/60	CPK≥1.67
Lead integrity	**LI**	C6						Not applicable, not a leadframe package
Test Group D – Die Fabrication Reliability Tests								
Electromigration	**EM**	D1	JP001A					Pass
Time dependent dielectric breakdown	**TDDB**	D2	JP001A					Pass
Hot carrier injection	**HCI**	D3	JP001A					Pass
Negative bias temperature instability	**NBTI**	D4	JP001A					Pass
Stress migration	**SM**	D5	JP001A					Pass

Table 7-1 Silicon reliability results (cont.)

Stress	ABV	Test#	Test method	Test conditions/Pre and Post ATE (Identify Temperature, RH, and Bias)	Requirements		Results	Comments
					S.S. per lot	# Lots	Fails/Total S.S.	
Test Group E – Electrical Verification Tests								
Pre- and post-stress electrical test	**TEST**	E1						Per pre and post ATE column
ESD - Human body model	**HBM**	E2	JS-001	Pass target ±1kV (Pre and Post ATE @ R & H)	12	1	0/36	
ESD - Charged device model	**CDM**	E3	JS-002	Pass target ±250kV (Pre and Post ATE @ R & H)	3	1	0/3	
Latch-up	**LU**	E4	JESD78	Ta=125°C (Class II) for SOV (1.5X Vop Max) and I-Test (±105mA) (Pre and Post ATE @ R & H)	6	1	0/6	
Electrical distributions	**ED**	E5						Not performed.
Fault grading	**FG**	E6						Available for review
Characterization	**CHAR**	E7						Not performed.
Electromagnetic compatibility	**EMC**	E9						Not performed. System level test
Short circuit characterization	**SC**	E10						Not applicable, not >12V or a power device
Soft error rate	**SER**	E11						Leverage Foundry simulation data

8 Revision history

Revision	Date	Description
AA	September 2024	Initial release
AB	March 2025	Table 4-3 QCS8300, QCS8275 PMIC device identification details: Added ES2 details for PMM8620AU
AC	October 2025	■ Table 4-3 *QCS8300, QCS8275 PMIC device identification details*: Added CS details for PMM8620AU ■ Table 4-4 *QCS9075 PMIC device identification details*: Added CS details for PMM8650AU

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