Qualcomm Technologies International, Ltd.

QCC711 Bluetooth Low Energy

Production Information Data Sheet

80-WL711-1 Rev. AH

March 14, 2025

Device description

- Low-power Single Mode Bluetooth® Low Energy SoC
- Bluetooth v5.4 specification
- Tri-core processor architecture including a dedicated processor for customer applications
- High security capabilities and services enabled by a true Root-of-Trust processor

Applications

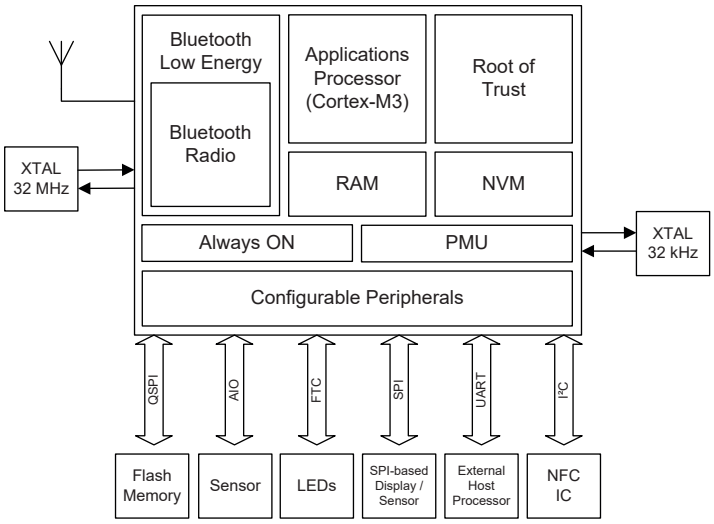
- Electronic shelf label (ESL) [a]
- Beacons
- Smart devices and accessories
- Smart home
- Building automation
- Wide range of Bluetooth Low Energy IoT

[a] ESL is restricted to licensed OEMs

Features

- Qualified to Bluetooth v5.4 specification
- Arm Cortex-M3 (32 MHz) Application Processor
- Arm Cortex-M0 (32 MHz) Bluetooth Processor
- 26 PIO
- Peripheral interfaces include: I²C, SPI, UART
- Flexible counter timer
- Quad SPI flash memory controller
- Analog I/O, battery voltage monitor, integrated temperature sensor
- Hosted and hostless modes
- Integrated PMU: 1.71 V to 3.6 V SMPS and LDOs
- 48-lead 5.6 mm x 5.6 mm x 0.85 mm, 0.4 mm pitch QFN

System architecture



QCC711 description

QCC711 is a low-power wireless single mode Bluetooth Low Energy SoC targeted at:

- Beacon applications for asset tracking and monitoring
- Smart devices and accessories for heath/fitness, remote control, computer peripherals
- Bluetooth on-boarding for Wi-Fi access points
- Smart homes for switches and sensors
- Building automation for monitoring and control
- A wide range of Bluetooth Low Energy IoT applications

Processors

QCC711 has dedicated processors with shared on-chip memory, SRAM and NVM, for Applications, Bluetooth Low Energy, and Root of Trust subsystems. The Applications subsystem uses an Arm Cortex-M3 processor for OEM application code. Code can run with or without an RTOS providing product designers with product customization flexibility.

Bluetooth

A dedicated Arm Cortex-M0 processor for the QCC711 Bluetooth subsystem executes the Bluetooth Low Energy stack in ROM, enabling consistent execution without processor resource competition. QCC711 supports Bluetooth v5.4 specification, single-mode Bluetooth Low Energy.

I/O (PIO)

QCC711 has a wide range of I/O and peripheral options available, including, QSPI, SPI, UART, I²C, FTC, and analog measurement. By employing these peripherals in various combinations, a wide range of applications are achievable.

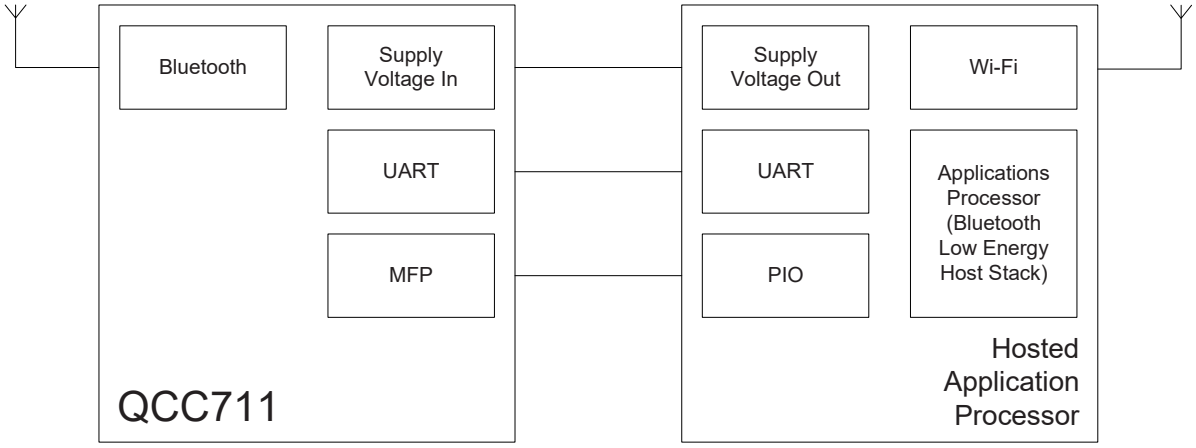
Software development tools

QCC711 is driven by a flexible software platform. For information on QCC711 development tools, Bluetooth, and other supported features, see CreatePoint.

QCC711 operating modes

QCC711 operates in one of two modes:

- **Hostless mode**: QCC711 is supplied directly from a battery, or an external regulator, and clocked from dedicated crystals. A sleep crystal offers lower system power to enable a longer battery life.
- **Hosted mode**: QCC711 connects to another hosted device using HCI over UART. For example, as shown in the following figure, an application processor device (access point). In this example, the Bluetooth Low Energy host stack is located in the application processor, which provides the voltage supply and uses the MFP for on/off control.



QCC711 connected in hosted mode

RELATED INFORMATION

"QCC711 example application schematic" on page 49

Ordering information

Device	Package			Order number
	Type	Size	Shipment method	
QCC711	QFN 48-lead (Pb free)	5.6 mm x 5.6 mm x 0.85 mm 0.4 mm pitch	Tape and reel	QCC-711-1-MQFN48C-TR-02-1 (v2.0) and QCC-711-1-MQFN48C-TR-03-1 (v2.1)

NOTE Your attention is drawn to QTIL's Terms of Supply, see http://www.qualcomm.com/salesterms or please request a copy), in particular the section covering Product Warranties and Disclaimers. Please note that the product warranty differs for production, pre-production, and other versions.

Production status minimum order quantity is 4 kpcs.

Supply chain: QTIL's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

QTIL contacts

General information	http://www.qualcomm.com
Sales information	qcsales@qti.qualcomm.com
Compliance and standards	product.compliance@qti.qualcomm.com

QCC711 device details

Bluetooth subsystem

- Arm Cortex-M0 (32 MHz) processor
- Qualified to Bluetooth v5.4 specification
  - Single mode Bluetooth Low Energy
  - Bluetooth Low Energy, advertising extensions, periodic advertising
  - 1 Mbps and 2 Mbps support
- Single ended antenna connection with on-chip balun and Tx/Rx switch
  - Tx power up to 7 dBm
  - Rx sensitivity -96 dBm
    - -99 dBm (boost) at 1 Mbps
- Bluetooth Low Energy Class 1 support

Application subsystem

- Arm Cortex-M3 (32 MHz) processor running OEM application code
- Timers/counters include 1 x 44-bit timer, 1 x 32-bit timer, low energy timer, and watchdog timer

Root-of-Trust subsystem

- RISC-V (32 MHz) processor
- QCC711 security feature controller, with hardware accelerators for AES, SHA, PKA, and PRNG

Shared access-controlled memory

- SRAM – 64 KB for customer application
- NVM – 384 KB for customer application

Clocks

- 32 MHz crystal (external)
- HFLPO (internal)
- 32 kHz crystal (external)
- LFLPO (internal)

Radio current consumption at 3 V

- Tx current consumption:
  - 9.9 mA at 0 dBm
  - 16.9 mA at 7 dBm
- Rx current consumption:
  - 4.6 mA at -98 dBm
- Sleeping power consumption between radio events (with 32 KB RAM retention and MCUs in Sleep state):
  - <2 µA

Power management

- Integrated power management unit (PMU)
- QCC711 runs directly from a 3 V coin-cell battery, supports (1.71 V to 3.6 V)
- Single switch-mode power supply (SMPS) and LDOs
- Battery brownout sensor
- Asynchronous wake events are not supported - for example from a PIO[a]
- Wake up from Sleep state using an interrupt on a PIO is not supported[a]

[a] Applies to (v2.0) only. For more details, see *QCC711 Bluetooth Low Energy Device Revision Guide* (80-WL711-4)

Security

- Root-of-Trust subsystem dedicated CPU provides secure execution environment
- Security capabilities:
  - General-purpose public key accelerator (PKA) with support:
    - NIST curves P-256, P-521
    - ECC Private/Public Key generation, ECDH, ECDSA
  - General-purpose symmetric crypto accelerator support:
    - AES128/256
    - SHA2-256/512
    - Crypto Block Cipher Modes (CBC, GCM, CTR)
    - MAC modes: HMAC-SHA2-256
  - Key Derivation Functionality (HKDF, RFC5869)
  - TRNG
- Security services:
  - Secure boot
  - Secure debug
  - Remote attestation
  - Secure provisioning
  - Secure communication and OTA-Firmware update

Debug and tools

- SWD and Segger debug support.
- IAR Embedded Workbench for Arm

Qualcomm Technologies Inc. (QTI) signature enabled, Root-of-Trust managed, system on-chip (SoC) specific keying material

- SoC specific keying material enables:
  - Device authentication: useful in distinguishing an authentic SoC device from one that is not (an unauthorized clone)
  - Remote attestation: enables an original equipment manufacturer (OEM) or service provider to determine the security state of the SoC at any given time
  - Onboarding: the process of delivering configuration data to a specific application device in the field
- SoC specific keying material as part of the QCC711 Root-of-Trust solution, is designed to create on demand:
  - a signed token encapsulating optional attestation statements
  - attestation and encryption public keys
  - a QTI signature: supplied at the time of SoC manufacturing

Peripherals and physical interfaces[a]

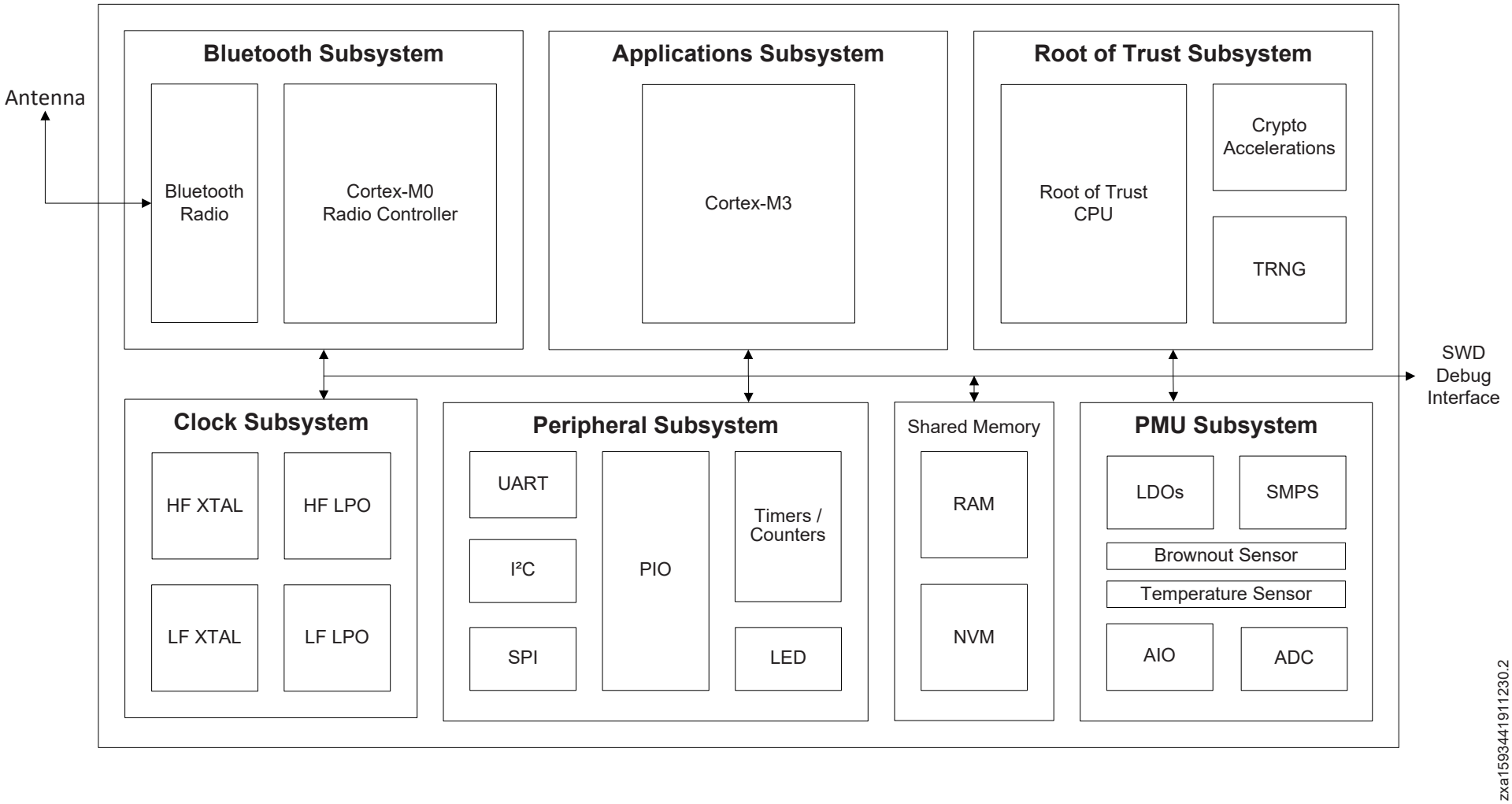
- 2 x SPI for SPI-based display/sensor (3-wire or 4-wire mode)
- 1 x SPI controller for external SPI flash memory (4 wire, or quad-mode 6 wire)
- 4 x FTC channels
- 4 x LED driver, combining FTC channels
- 3 x UART for Application subsystem (2 x 9-bit and 1 x 8-bit)
- 2 x I²C controller-only interfaces for EEPROM and/or NFC, or other I²C peripherals
- 1 x I²C peripheral-only interface
- 26 x PIO, 4 of which have analog capability
- 2 x AIO inputs for ambient light sensor
- 1 x ADC (10-bit, 0 V to 3.6 V range or 0 V to 1.8 V range)
- 2 x Voltage comparators; to separately monitor battery voltage level during application processor activity or radio Tx operation
- 1 x MFP input-only; software configurable
- Internal temperature sensor

Package and compliance

- 48-lead 5.6 mm x 5.6 mm x 0.85 mm, 0.4 mm pitch QFN
- Temperature range -40 to 85 °C
- Green (restriction of hazardous substances (RoHS) compliant, and no antimony or halogenated flame retardants)

[a] Not all interfaces are available concurrently; some combinations are excluded.

QCC711 functional block diagram



QCC711 functional block diagram

Revision history

Revision	Date	Change reason
AA	December 2021	Updated with v2.0 silicon updates to Document title, Front page, Ordering information, Device details, and Sections 1.1, 2.2, 3.8, 6, 7, 8.4.3, 8.4.4, 9.1, 9.2, 11.4, 11.7, 12, 13.1, 13.5, 13.6, 14.1, 14.2, 15.1, 15.2, 15.3, 18.3.2, 19, 19.1, and Glossary.
AB	October 2022	Updates to Front page, Description, Ordering information, Device details, and Sections 1.1, 1.2, 1.5, 1.6, 2, 2.1, 4.3, 8.4, 8.4.2, 9.1, 9.2, 11, 12, 14, 14.1, 14.2, 15, 15.1, 15.2, 15.3, 19, 19.1, 19.2, and Document references, and Glossary.
AC	December 2022	Update to Section 19.1.
AD	July 2023	Updated to QCC711 throughout. Updates to Front page, Description, Ordering information, Device details, and Sections 1.1, 2, 8.1, 13.2, 15, 15.1, 15.3, 19, 19.1, 19.2, and Document references, and Glossary.
AE	August 2023	Updated to Production Information status (v2.0).
AF	September 2023	Updated to Production Information status (v2.1).
AG	January 2024	Minor editorial updates.
AH	March 2025	Editorial updates.

Status information

QTIL Product Data Sheets progress according to the following formats: Advance Information, Engineering Sample, Pre-production Information, and Production Information. The status of this document is **Production Information**.

Advance Information

Information for designers concerning QTIL product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

Engineering Sample

Information about initial devices. Devices are untested or partially tested prototypes, their status is described in an Engineering Sample Release Note. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by QTIL without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalized. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by QTIL without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

Device implementation

As the feature-set of the QCC711 is firmware build-specific, see the relevant software release note for the exact implementation of features on the QCC711.

Life support policy and use in safety-critical applications

QTIL products are not authorized for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. QTIL will not warrant the use of its devices in such applications.

Contents

Tables

Figures

1 Package information

QCC711 is available in a 5.6 mm x 5.6 mm x 0.85 mm 48-lead QFN package.

1.1 Chip marking

Chip marking identifies lot-specific information about QCC711.

Figure 1-1 shows the product marking for QCC-711-1-MQFN48C-TR-02-1 (v2.0) and QCC-711-1-MQFN48C-TR-03-1 (v2.1) in a 48-lead 5.6 mm x 5.6 mm x 0.85 mm QFN package.

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Figure 1-1 QCC711 chip marking

NOTE Figure 1-1 is not to scale. The marking font and image are for illustration purposes only.

The circle location mark identifies lead 1.

Table 1-1 QCC711 chip marking content

Line	Description	Definition
1	Qualcomm text	-
2	Product name	QCC711
3	Config, revision, and feature codes	102 (v.2.0) 103 (v2.1)
OPTIONAL	Space for optional trace information; can be 1 or more lines	-
4	Manufacturing trace code	AYWWXXX ■ A: Assembly site code ■ Y: Year ■ WW: Work week ■ XXX: Lot serial number

1.2 QCC711 package dimensions diagram

Figure 1-2 shows the dimensions of the QCC711 package from top, bottom, and side views.

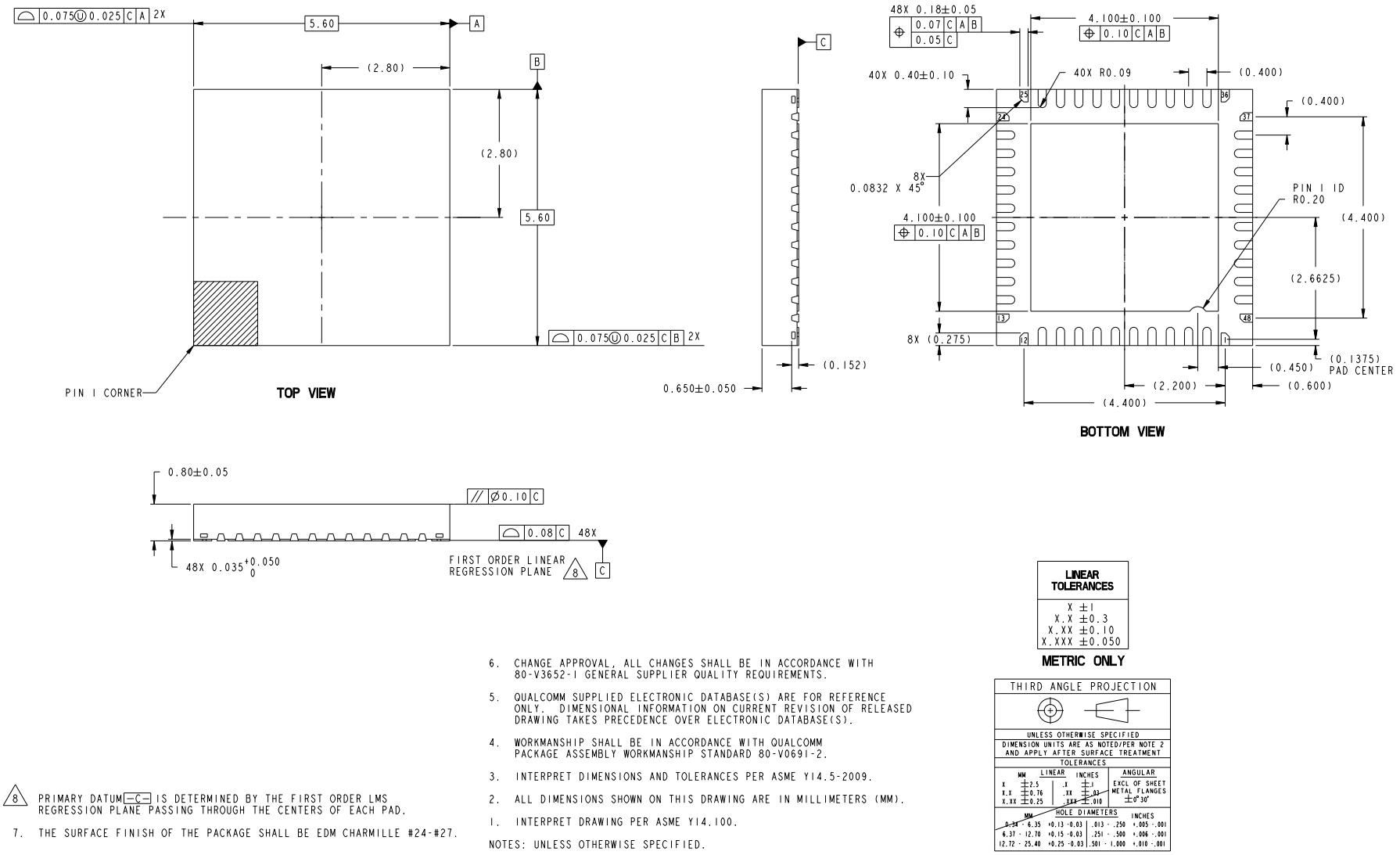

Figure 1-2 QCC711 package dimensions diagram

1.3 QCC711 lead allocations

QCC711 has a 48-lead QFN package. Lead 25 (VSS) and the ground paddle are used for electrical grounding, mechanical strength, and thermal continuity. Figure 1-3 shows QCC711 lead allocations.

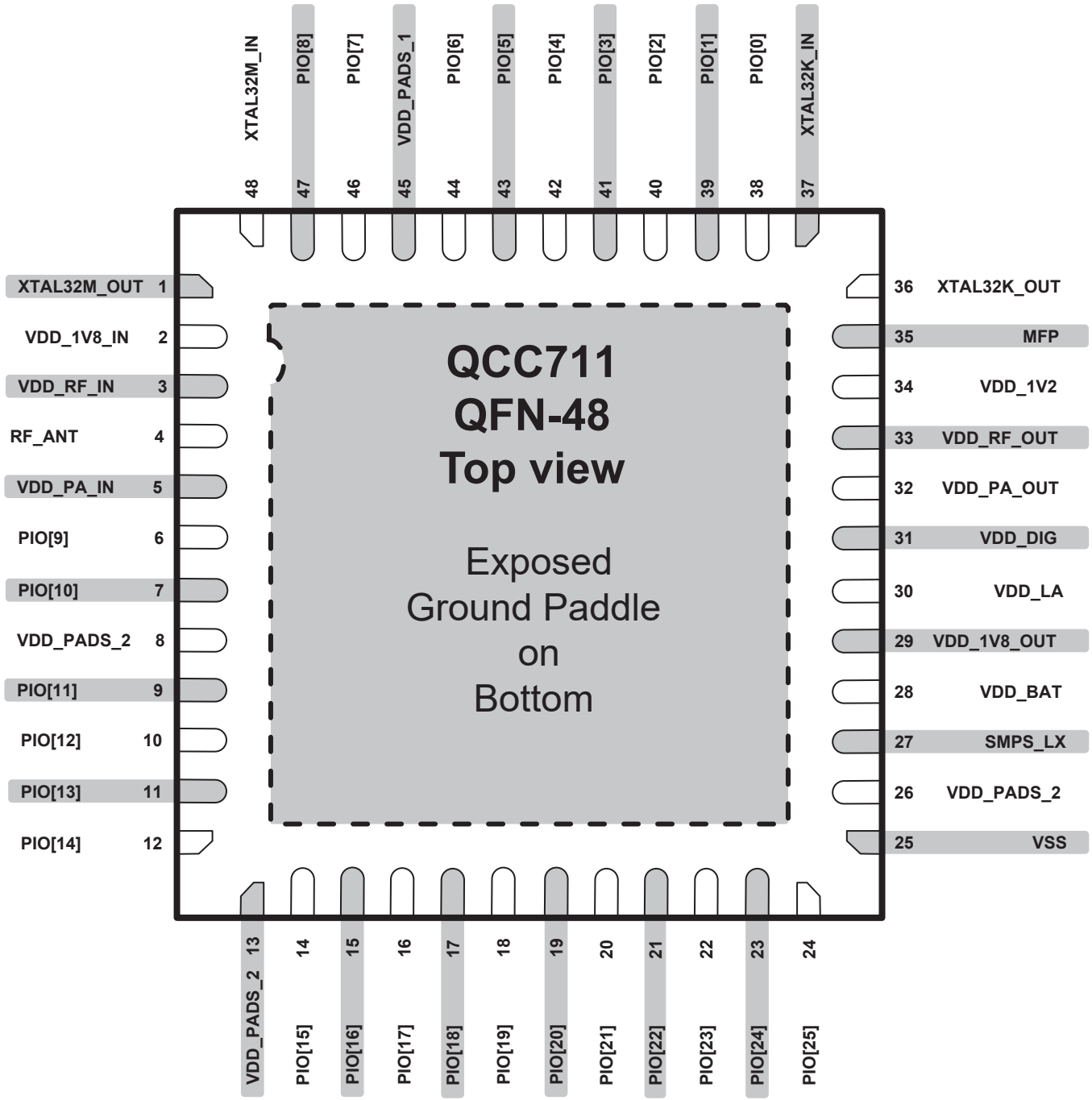

Figure 1-3 QCC711 lead allocations (orientation from top of device)

1.4 QCC711 device terminal functions

The leads on the QCC711 are grouped into various terminal functions. The device terminal functions include:

- Radio
- Clock
- PIO
- Control
- Power supplies
- Ground

Table 1-2 lists pad type definitions for the device terminal functions.

Table 1-2 Pad type definitions for device terminal functions

Symbol	Description	Symbol	Description
AI	Analog input	P	Voltage supply
AO	Analog output	Z	High-impedance (high-Z) output
AIO	Analog input or output	OD	Open Drain
DIO	Bidirectional digital	**Pad pull details for digital I/O**	
DI	Digital input	PU	Input signals with weak internal pull-up, to prevent signals from floating when left open
DO	Digital output	PD	Input signals with weak internal pull-down, to prevent signals from floating when left open
GND	Ground	NP	Contains no internal pull
NC	No connection		

1.4.1 Radio device terminal functions

Table 1-3 QCC711 Radio device terminal functions

Signal name	Lead number	Pad type	Power domain	Description
RF_ANT	4	RF	-	Bluetooth transmit/receive.

1.4.2 Clock device terminal functions

Table 1-4 QCC711 Clock device terminal functions

Signal name	Lead number	Pad type	Power domain	Description
XTAL32K_IN	37	AI	-	XTAL input for 32.768 kHz clock.
XTAL32K_OUT	36	AO	-	XTAL output for 32.768 kHz clock.
XTAL32M_IN	48	AI	-	XTAL input for 32 MHz clock.
XTAL32M_OUT	1	AO	-	XTAL output for 32 MHz clock.

1.4.3 PIO device terminal functions

PIOs have different states according to the power or reset state of the device.

QCC711 reset states

- **POR_RST_A**: a power on reset (POR) from the on-chip power management unit (PMU) in hostless mode. The POR sequence is triggered in response to a battery attach event **before** the core supply is stable.
- **POR_RST_B**: a POR from the on-chip PMU in hostless mode. The POR sequence is triggered in response to a battery attach event **after** the core supply is stable.
- **COLD_RST**: similar to a POR. A cold reset causes a full power OFF/ON sequence, and can be triggered by:
  - software requests
  - a watchdog bite event (in mission mode)
  - a brownout event
  - a multi-function pin (MFP) input >10 s
- **WARM_RST**: this reset is triggered **before** the chip enters Low Power mode.

Table 1-5 QCC711 PIO power supply and reset definitions

PIO port	Power domain	POR_RST_A	POR_RST_B	COLD_RST	WARM_RST
PIO[25:11]	VDD_PADS_2	Hi-Z	Weak pull down	Weak pull down	Latched[a]
PIO[10]	VDD_PADS_2	Hi-Z	SWD_DIO	SWD_DIO	Latched[a]
PIO[9]	VDD_PADS_2	Hi-Z	SWD_CLK	SWD_CLK	Latched[a]
PIO[8:0]	VDD_PADS_1	Hi-Z	Weak pull down	Weak pull down	Latched[a]

[a] In WARM_RST state, all PADs are latched to the state before QCC711 enters Low Power mode.

NOTE QCC711 PIOs have extensive multiplexing capabilities to access numerous digital peripherals. For details, see *Related Information*.

Table 1-6 QCC711 PIO device terminal functions

Signal name	Lead number	Pad type	Power domain	Description
PIO[25]	24	DIO / AI	VDD_PADS_2	Generic PIO, Analog inputs configurable
PIO[24]	23	DIO / AI	VDD_PADS_2	Generic PIO, Analog inputs configurable
PIO[23]	22	DIO / AI	VDD_PADS_2	Generic PIO, Analog inputs configurable
PIO[22]	21	DIO / AI	VDD_PADS_2	Generic PIO, Analog inputs configurable
PIO[21]	20	DIO	VDD_PADS_2	Generic PIO
PIO[20]	19	DIO	VDD_PADS_2	Generic PIO
PIO[19]	18	DIO	VDD_PADS_2	Generic PIO
PIO[18]	17	DIO	VDD_PADS_2	Generic PIO
PIO[17]	16	DIO	VDD_PADS_2	Generic PIO
PIO[16]	15	DIO	VDD_PADS_2	Generic PIO
PIO[15]	14	DIO	VDD_PADS_2	Generic PIO
PIO[14]	12	DIO	VDD_PADS_2	Generic PIO
PIO[13]	11	DIO	VDD_PADS_2	Generic PIO
PIO[12]	10	DIO	VDD_PADS_2	Generic PIO
PIO[11]	9	DIO	VDD_PADS_2	Generic PIO
PIO[10]	7	DIO	VDD_PADS_2	Generic PIO
PIO[9]	6	DIO	VDD_PADS_2	Generic PIO
PIO[8]	47	DIO	VDD_PADS_1	Generic PIO
PIO[7]	46	DIO	VDD_PADS_1	Generic PIO
PIO[6]	44	DIO	VDD_PADS_1	Generic PIO
PIO[5]	43	DIO	VDD_PADS_1	Generic PIO
PIO[4]	42	DIO	VDD_PADS_1	Generic PIO
PIO[3]	41	DIO	VDD_PADS_1	Generic PIO
PIO[2]	40	DIO	VDD_PADS_1	Generic PIO
PIO[1]	39	DIO	VDD_PADS_1	Generic PIO
PIO[0]	38	DIO	VDD_PADS_1	Generic PIO

RELATED INFORMATION

"PIO" on page 40

1.4.4 Control device terminal functions

Table 1-7 QCC711 control device terminal functions

Signal name	Lead number	Pad type	Power domain	Description
MFP	35	DI	VBAT	Multi-function pin and software configurable as a reset input.

1.4.5 Power supply device terminal functions

Table 1-8 QCC711 Power supply device terminal functions

Signal name	Lead number	Pad type	Power domain	Description
SMPS_LX	27	AO	-	Inductor connection for the Buck SMPS.
VDD_1V2	34	P	-	1.2 V supply for internal PMU control circuit and 32.768 kHz XTAL. An external 470 nF decouple capacitor is recommended.
VDD_1V8_IN	2	P	-	Supply for 32 MHz XTAL and SAR ADC. Connect directly to VDD_1V8_OUT (Lead 29) using PCB trace. An external 10 nF decouple capacitor is recommended.
VDD_1V8_OUT	29	P	-	1.8 V supply for 32 MHz XTAL and SAR ADC. An external 470 nF decouple capacitor is recommended.
VDD_BAT	28	P	-	Battery voltage input. Two 0603-size external 10 µF capacitors are recommended.
VDD_DIG	31	P	-	1.1 V supply for digits core power. An external 470 nF decouple capacitor is recommended.
VDD_LA	30	P	-	1.35 V supply to the system. A 0603-size external 10 µF decouple capacitor is recommended.
VDD_PA_IN	5	P	-	Supply for Bluetooth power amplifier. Connect directly to VDD_PA_OUT (Lead 32) using PCB trace. An external 10 nF decouple capacitor is recommended.
VDD_PA_OUT	32	P	-	1.15 V supply for Bluetooth power amplifier. An external 470 nF decouple capacitor is recommended.
VDD_PADS_1	45	P	-	Power domain for PIO [8:0]. An external 100 nF decouple capacitor is recommended.
VDD_PADS_2	8, 13, 26	P	-	Power domain for PIO [25:9]. An external 100 nF decouple capacitor is recommended for each lead.
VDD_RF_IN	3	P	-	Supply for Bluetooth radio. Connect directly to VDD_RF_OUT (Lead 33) using PCB trace. An external 10 nF decouple capacitor is recommended.
VDD_RF_OUT	33	P	-	1.1 V supply for Bluetooth radio. An external 470 nF decouple capacitor is recommended..

1.4.6 Ground device terminal functions

Table 1-9 QCC711 Ground device terminal functions

Signal name	Lead number	Pad type	Power domain	Description
VSS	25, Ground Paddle	GND	-	Ground.

1.5 QCC711 PCB design and assembly considerations

Recommendations to achieve maximum board-level reliability of the QCC711 IC package.

- Use of nonsolder mask defined (NSMD) lands (lands smaller than the solder mask aperture) are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With

solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.

- Qualcomm Technologies International, Ltd. (QTIL) recommends that the printed circuit board (PCB) land pattern is in accordance with Institute of Printed Circuits (IPC) standard IPC-7351B.
- Solder paste must be used during the assembly process.

For more information about QCC711 PCB design, see *QCC711 Hardware Design Guide* (80-WL711-5).

1.5.1 Typical solder reflow profile

For further information describing the reflow profile of an integrated circuit (IC) when attaching its physical connection solder points to a PCB see *Typical Solder Reflow Profile for Lead-free Devices Information Note* (80-CT462-1).

1.6 Moisture sensitivity level

QCC711 is qualified to moisture sensitivity (MSL3) in accordance with JEDEC J-STD-020.

2 Bluetooth subsystem

The Bluetooth subsystem is a single-mode radio supporting Bluetooth Low Energy.

The Bluetooth subsystem is fully qualified to the Bluetooth v5.4 specification. It has:

- 32 MHz Arm Ltd. (Arm) Cortex-M0 processor running Bluetooth firmware
- Bluetooth packet processing engine and modem
- Power and clocks automatically removed to reduce power when the Bluetooth radio is not operating

2.1 Bluetooth v5.4

QCC711 supports Bluetooth Low Energy to the Bluetooth v5.4 specification.

2.2 Bluetooth radio

The Bluetooth radio consists of a single radio frequency (RF) input/output (I/O) port shared for receive and transmit. The RF port impedance is 50 Ω when operating.

3 Crystal oscillator

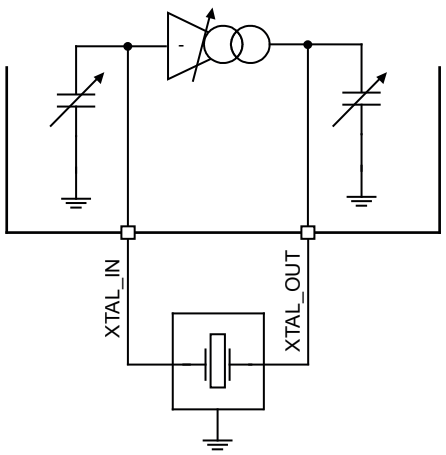

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Figure 3-1 Crystal oscillator

The Bluetooth specification requires frequency accuracy of ±40 ppm. The output RF frequency is directly linked to the frequency accuracy of the crystal oscillator, so this must be ±40 ppm. This specification is required over the operating temperature of the device.

NOTE The crystal is specified by the following terms:

- Initial Frequency Error: The difference between the required frequency and the actual oscillating frequency caused by the crystal and its PCB connections. It is also called Calibration Tolerance or Frequency Tolerance
- Frequency Stability Error: The total of how far the crystal can move off frequency with temperature, aging, or other effects. It is also called Temperature Stability, Frequency Stability, or Aging.
- Pullability: The change in frequency for a change in load capacitance.

QCC711 contains an array of internal capacitors attachable to the XTAL_IN and XTAL_OUT nodes. These can be switched to pull the crystal onto frequency and compensate for initial frequency errors by using a simple per-device trim on the production line. The trim is stored in the Application subsystem. It is not possible to compensate for frequency stability errors. A crystal should be chosen with a frequency stability error better than the Bluetooth specification ±40 ppm clock accuracy.

Some crystal data sheets combine both these terms into one tolerance value. This results in compensation of only the initial frequency error and a trim that does not compensate for temperature or aging performance. If frequency stability is not explicitly stated, QTIL cannot guarantee remaining within the Bluetooth's ±40 ppm frequency accuracy specification.

The sum of Initial Frequency Error and Frequency Stability Error must be kept below the Bluetooth specification of ±40 ppm. Typically use a crystal with ±15 ppm frequency stability over temperature/aging.

To improve startup time and achieve minimum current consumption, crystals with low capacitive loading are preferred. However, this may result in greater susceptibility to environmental frequency variation.

3.1 LPO CAL

LPO CAL is used to measure the frequency of another clock relative to a 32 MHz crystal. The control logic starts a counter running on a fast, accurate clock domain, and counts over a programmed number of edges of the target clock. Countval is divided by the number of edges over which the measurement is taken.

Measurement accuracy:

- Slow Clock: Using the fast clock to measure the slow clock introduces an error at the start and end of the measurement. With a slow edge counter of 800 every clock from ideal, can be shown to equate to 1.25 ppm of inaccuracy.
- Fast Clock: To measure a fast clock, it is necessary to scale the clock to ensure that no edges are missed when the edge count is taken. Therefore the measured clock is prescaled first. Over L clocks we can show the resolution ppm to be:

  ```
  Resolution = (ClkMes / Scaling) / Counter x 32 MHz
  ```

3.2 32.768 kHz crystal

The QCC711 32.768 kHz crystal oscillator is used for:

- accurate wake up
- Bluetooth Low Energy sleep clock

A low power 32 kHz crystal oscillator is needed for timing in sleep modes. Matching load capacitances are provided on chip that support tuning of crystals requiring matching load capacitance from 4 pF to 12.5 pF. Lower current consumption is achieved with a smaller load capacitance crystal.

The system requires trimming to (32.768 kHz) better than 4 ppm with the onboard adjustable load capacitance (oscillator, an array of internal capacitors attachable to the XTAL_IN and XTAL_OUT nodes, 35 fF effective steps) and compensated for initial frequency errors using a simple per-device trim on the production line at room temperature.

Frequency pullability depends on the matching load capacitance of the crystal. Current consumption also depends on the equivalent series resistance (ESR) of the crystal – a smaller ESR gives lower consumption.

At the same time as the frequency trim, the crystal type (setting based on load cap and ESRmax) must be loaded to resistive random-access memory (RRAM), to ensure correct operation, and minimize operating current; before running the crystal. Parasitic capacitance on the PCB to the crystal must be minimized to allow tuning of the crystal (particularly for small load capacitance crystals). It must be below 3 pF per terminal for 4 pF crystals, and 4 pF per terminal for 6 pF and larger crystals. Of this capacitance, less than 0.2 pF may be shunt capacitance (between XTAL_IN and XTAL_OUT).

3.3 32 MHz crystal

The QCC711 32 MHz crystal oscillator is used for:

- RF activity
- UART baud clock
- for running applications when Bluetooth Low Energy is not awake

Any of the three subsystems can request the use of the 32 MHz crystal oscillator as the high frequency clock source; this is as opposed to the alternate, lower accuracy internal high frequency low-power oscillator (HFLPO).

This crystal oscillator is automatically powered off and deselected when the system on-chip (SoC) goes into Sleep or Hibernate state, at which time the SoC switches to its internal low frequency low-power oscillator (LFLPO). Both the oscillator choice and the configuration of the oscillator, persist across low power states, and are automatically restored when the SoC wakes up into Active state.

The management of the oscillator is automated and software is relieved of most monitoring tasks. Ordinarily, software only needs to select a clock source and the hardware manages all other items of concern.

3.4 Global clock controller

The global clock controller (GCC) is responsible for clock and reset distribution for different subsystems. Clock gates are inserted in front of each subsystem, to gate the clock off near clock origin, and to reduce dynamic power consumption whenever the subsystem is not needed.

The GCC has an internal hardware finite state machine (FSM) that triggers the start-up sequence for the 32 MHz crystal when requested, after exiting from QCC711 Sleep state.

3.4.1 Timers

A 44-bit global timer and a 32-bit central timer (with capture and compare capabilities) are available. The global timer provides 1 µs resolution at 16 MHz (effective update rate).

The central timer block provides 12 different microsecond resolution comparators that can be mapped to any of the interrupt lines to the Applications subsystem. Hardware can detect when firmware is late (within a certain time) when programming a compare value, and generating a corresponding interrupt. The actual time is captured in memory mapped registers. A closest-in-time circuit provides information on which enabled comparator matches next.

Configurable timer capture mechanisms are provided to capture certain external trigger or internal firmware events.

3.5 32.768 kHz crystal performance specification

Table 3-1 lists 32.768 kHz crystal performance specification for QCC711.

NOTE Performance to be met over operating temperature range unless otherwise stated.

Table 3-1 QCC711 32.768 kHz crystal specification

Parameter	Min	Typ	Max	Units	Notes
Operating frequency	-	32.768	-	kHz	-
Mode of Vibration	Fundamental				AT-cut fundamental.
Initial frequency tolerance	-20	-	20	ppm	25°C ± 3°C.
Turnover	20	25	30	°C	-
Parabolic coefficient	-0.04	-	-	ppm/°C^2	-
Aging	-	-	3	ppm/year	-
Operating temperature	-40	-	85	°C	-
Storage temperature	-40	-	125	°C	-
Equivalent series resistance	-	-	90	kΩ	-
Motional capacitance	0.6	-	10	fF	-
Shunt capacitance	-	-	1.5	pF	-
Load capacitance	4	-	12.5	pF	-
Drive Level	-	-	1	µW	-
Insulation resistance	500	-	-	MΩ (100 V)	-

3.6 32.768 kHz crystal selection considerations

Best power consumption is obtained by using a crystal with the lowest possible matching load capacitance and ESR. This permits a lower drive level setting of the driver circuit. The expectation is that changing from a typical 6 pF to 4 pF load capacitance crystal, could save approximately 28 nA in Sleep state. Optimal power consumption is obtained with a crystal with a 4 pF capacitance load.

3.7 32 MHz crystal performance specification

Table 3-2 lists performance to be met over operating temperature range unless otherwise stated.

Table 3-2 Electrical requirements

Parameter	Description	Min	Typ	Max	Units	Notes
F_{nom}	Nominal fundamental frequency	-	32	-	MHz	-
C_P	Package capacitance (32 MHz)	-	1	2	pF	-
C_L	Load capacitance	-	6	10	pF	-
F_tol_nom	Frequency tolerance nominal	-10	-	10	ppm	At 25°C ± 3°C
F_tol_temp	Frequency stability over temperature	-10	-	10	ppm	Over specified temperature range with respect to frequency error at nominal
F_tol_aging	Frequency tolerance with aging at Ta = 25°C ± 3°C	-1	-	1	ppm/yr	1st year
F_tol_aging_10yrs	Total frequency tolerance with aging over 10 years	-10	-	10	ppm	-
ESR	Motional Resistance (32 MHz)	-	25	50	Ω	-
Drive Level	DL	-	100	200	µW	-

3.8 32 MHz crystal selection considerations

To meet the Bluetooth specification, it is important that the frequency tolerance of the 32 MHz clock stays within ±40 ppm for the lifetime of the product. A customer should remove initial frequency error at production test, by adjusting load capacitors. Load capacitor adjustment removes error introduced by the crystal, assembly, and parasitics; particularly for board and chip pin. Remaining tolerance should be provided to handle the effects of temperature and aging.

4 System power states

The Always ON (AON) module provides the minimum digital functionality required to remain operational in the lowest power modes, as well as a number of not-always-on (NAON) functions. The power management engine (PME) provides always-on control of device boot and provides control of power state, clocks and resets, and memory retention based on requests from firmware.

Figure 4-1 shows QCC711 power states.

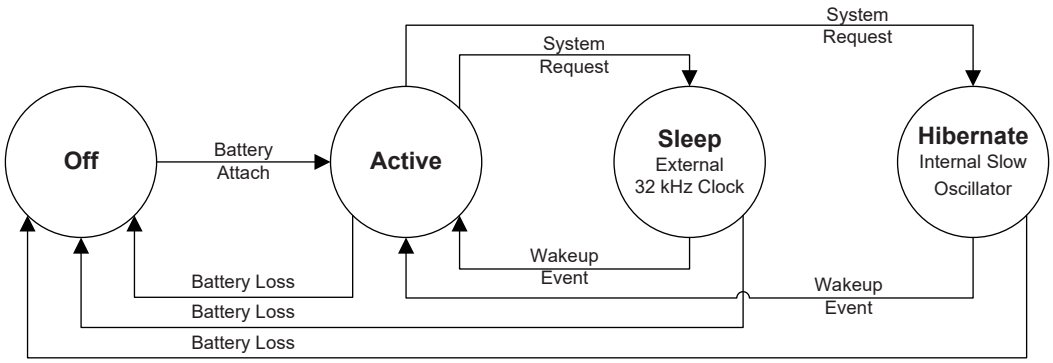

Figure 4-1 QCC711 power states diagram

In Off state the SoC is not powered. The lowest power consumption state is Hibernate, followed by Sleep and then Active.

The SoC can automatically adjusting its power state with minimum intervention from subsystem software. The SoC automatically moves into its lowest power consumption state, consistent with subsystem requirements, as expressed by the subsystem software through a set of voting registers.

4.1 Off state

In Off state, no battery is attached, and QCC711 is inert. When a battery is attached, QCC711 transitions to Active state automatically.

4.2 Active state

In Active state, the main power domain is powered on and subsystems can operate normally.

In Active state, the chip runs subsystem software as determined by the configuration requested by software. In the most common case of an operative chip, in this state, the SoC runs software on one or more of its three subsystems. As soon as all three subsystems request to be put in low power mode, the SoC as a whole transitions into Sleep or Hibernate state, depending on software preference.

4.3 Sleep state

In Sleep state most of the SoC is powered off. The SoC remains capable of waking up into Active state under a number of conditions.

If enabled the 32 kHz crystal remains running and continues to be used as the time reference clock.

In particular, it is possible to program an accurate wake-up time for the Applications and/or the Bluetooth subsystem, with precisions compatible with the timing needs of Bluetooth protocols.

In Sleep state the SoC tracks real time.

4.4 Hibernate state

In Hibernate state the SoC powers down as much logic as possible while still retaining a certain amount of configuration and the capability to wake up.

In this state, timed wake-ups can be programmed as in Sleep state but with far lower accuracy. And the SoC loses the ability to track real time with usable accuracy.

5 Applications subsystem

The QCC711 Applications subsystem provides a processor and resources for customer application code execution.

5.1 Application subsystem features

The QCC711 Application subsystem features:

- a 32 MHz Arm Cortex-M3 processor for customer execution that features memory protection logic and can execute code with or without a real-time operating system (RTOS)
- non-volatile memory (NVM) for program storage, using on-chip RRAM
- peripheral interface control of universal asynchronous receiver transmitter (UART), inter-integrated circuit interface (I²C), and serial peripheral interface (SPI)
- bit-banding access to top-level mode multiplexing (TLMM) registers
- Arm CoreSight debugger support
- 4-bit trace port and single wire output (SWO) support
- address remapping for NVM and static random access memory (SRAM) boot support
- boot address offset support within NVM and SRAM regions
- Sleep and Power-down modes support

6 SRAM module

The SRAM module provides a pool of SRAM memory shared between Bluetooth (M0), Applications (M3), and Root of Trust subsystem processors. Memory allocation is flexible and runtime configurable.

QCC711 has a total of 128 KB of SRAM for these subsystems. This memory is configured as 16 memory blocks of 8 KB each:

- 32 KB for retention support
- remaining 96 KB is power collapsed in QCC711 Sleep state

Up to 64 KB (of the 128 KB) is available for customer applications:

- 16 KB for retention support
- 8 KB shared between M0 and M3
- 40 KB for any use - with repartition between shared and customer specific usage (adjustable in blocks of 8 KB)

7 NVM module

The NVM module provides 512 KB of shared RRAM memory to the system.

The NVM presents a memory divided into regions, to support multiple subsystems. The NVM module uses an embedded 4 Mb RRAM.

Memory is divided into 16 regions, with each region having its own access control settings. These regions are under Qualcomm or customer control.

The NVM is a single resource, with multiple subsystems accessing it. The Root of Trust (RoT) subsystem is the owner of the NVM and configures it by setting region allocation and access control. When the NVM is configured, subsystems have read access to their respective memory regions. The RoT does not need to manage read access from the subsystems. When a subsystem wants to write to a memory region, the RoT allocates NVM module functions to the subsystem, and the subsystem writes to the memory. The subsystem can manage its own access control to the allocated memory regions.

The 512 KB of shared RRAM memory is allocated:

- 64 KB for M0
- 64 KB for RoT
- 384 KB for customer applications

  NOTE This 384 KB is for both code and data; in particular data for OTA-U (as required).

8 Peripheral module

Figure 8-1 shows the QCC711 peripheral module.

The primary purpose of the Peripheral module is to provide interfaces for customer application use and control from the Applications subsystem.

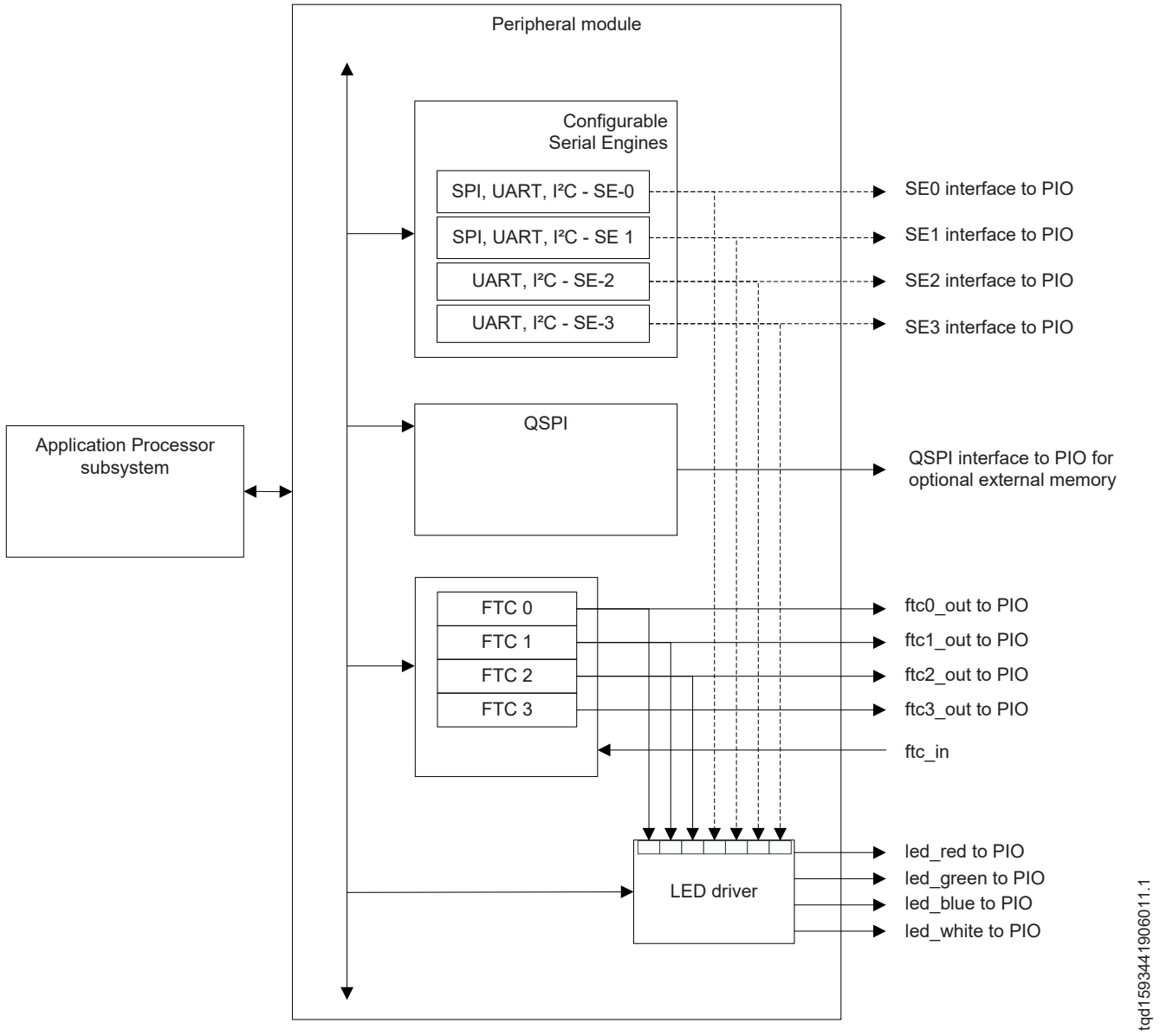

Figure 8-1 QCC711 Peripheral module

8.1 Peripheral module features

The QCC711 Peripheral module incorporates different controller and peripheral intellectual property (IP)s for certain use cases. It includes integrated direct memory access (DMA) that supports both transfers to and from peripheral interfaces, and memory-to-memory transfers. Table 8-1 lists the peripherals available for QCC711.

Table 8-1 QCC711 peripheral IPs

Components	High-level specification
QSPI controller	■ used for external flash ■ configurable controller and peripheral SPI ■ 4-wire/8-bit standard interface ■ slower clock rate operation support ■ dual/quad SPI support
FTC	■ application timer and light-emitting diode (LED) pattern driving capability supported ■ up to 4 timer/counter instantiations
LED pattern generator	-
SEs / QUPs offer the following capabilities:	
3 x UART	■ up to 2 Mbaud maximum UART rate capability ■ 8-bit and 9-bit mode ■ 2x UARTs support 9-bit data transfer mode ■ hardware flow control ■ DMA to / from system memory to reduce first-in first-out (FIFO) size and processor load ■ programmable fractional baud rate generation from 32 MHz system clock
2 x I²C controllers	■ controller SM, FM, and FM+ external pull-up resistors ■ 100 kbps, 400 kbps, and 1000 kbps rates ■ external pull-up resistors required ■ DMA to/from system memory to reduce FIFO size and processor load
SPI controllers	■ configurable 3-wire / 9-bit mode and 4-wire / 8-bit mode ■ compatible with SPI-based display/sensor interfaces ■ slower clock rate operation supported ■ 3-wire and 4-wire SPI for display supported by serial engine (SE) 0 ■ true 4-wire SPI □ capable of concurrent operation, with DMA support □ clock divider for lower frequency operation with limited capability devices □ 4-wire 8-bit controller mode for external flash, other SPI-based displays/sensors, and standard peripherals □ 4-wire 8-bit SPI peripheral mode □ 32-bit mode with DMA, for arbitrary pattern generation from memory under application firmware control - output of this SPI mode may be connected to FTC inputs for extra application flexibility to drive LED patterns
DMA	■ date size: 8-bit, 16-bit, and 32-bit supported ■ DMA transfer types between memories and peripherals supported

8.2 QSPI controller

The QCC711 quad serial peripheral interface (QSPI) controller:

- supports dual/quad SPI mode for higher performance data transfer capability
- execution in place is not supported on this interface

8.3 Flexible timer/counter

The QCC711 has four flexible timer/counter (FTC) blocks, this is a common function that is found in almost all mixed signal microcontrollers.

Each FTC block has the following main features:

- application timer and LED pattern driving capability with up to four timer/counter instantiations
- support for LED pattern-flashing
- 16-bit counter/timer
- various operating modes:
  - count up, down or up-down
  - single shot or continuous
  - free running from clock source or gated
  - edge, signed, and triggered count modes
- configurable clock sources:
  - internal clock
  - external clock from a pad with optional gating, clocked on rising, falling or both edges
  - count on multiple input clocks (for quadrature encoder behavior)
  - cascaded from another FTC block for longer than 16-bit counters
- 16-bit programmable counter clock prescaler
- auto-reload register (counter maximum value)
- 3 capture/compare channels (configurable as input capture or compare/pulse width modulation (PWM))
- configurable noise filter on inputs
- flexible counter event control, enabling the following input measurement/capture functions:
  - clock period measurement
  - pulse width measurement

    - quadrature decoder (X1, X2, X4 decoding types)
    - the preceding functions are achieved through the following counter event control features:
        - start, stop, increment, decrement, and clear events individually triggerable by:
            - register write
            - programmable input/output (PIO)
            - overflow of previous cascaded FTC block
        - event edge detection:
            - rising edge
            - falling edge
            - either edge
            - neither edge (disabled)

- multiple output waveform generators, enabling complex output waveform generation:
    - multiple PWM outputs with optional dead time between outputs for driving motor bridges
    - variable frequency generation
    - the preceding functions are achieved through the following output generation control features:
        - match with comparator/s, maximum value reached, zero value reached, and manually triggered events that control the output behavior as follows:
            - toggle output
            - set output high
            - reset output low
            - unchanged (disabled)

- interrupt generation on the following events:
    - counter overflow/underflow
    - input capture
    - capture overflow
    - compare match
    - trigger event (counter start / stop / init by internal / external trigger)
- programmable operation during debug mode

8.4 QCC711 serial engines and supported interfaces

QCC711 has four programmable SE / Qualcomm universal peripheral (QUP) that are configurable for serial interfaces, such as SPI, UART, or I²C, see Table 8-2.

Table 8-2 QCC711 serial engines and supported interfaces

SE/QUP	3-wire or 4-wire SPI display controller	True 4-wire SPI controller/ peripheral	I²C controller	UART	9-bit UART	DMA
SE0	Yes	Yes	Yes	Yes	Yes	Yes
SE1	Yes	Yes	Yes	Yes	Yes	Yes
SE2	No	No	Yes	Yes	No	Yes
SE3	No	No	Yes	Yes	No	Yes

Each SE has five output ports. The functions of these ports are specific to each of the selected interfaces. Table 8-3 lists the port feature mapping. The following section shows how these ports can be routed as sets to different physical PIOs. As such, the ports of each SE are presented as numerous copies to the top level multiplex. Alternative copies must be used as a complete block, this restriction keeps the physical interface grouped to adjacent PIOs.

The SEs that Table 8-3 lists have default port mappings for the different types of interface, see Table 8-3.

Table 8-3 Default port mappings for QCC711 serial engines

Default SE port mapping	3-wire SPI display	4-wire SPI display	I²C	UART	SE0 true 4-wire SPI
Port 0	CS1	CS1	SDA	CTS	MISO
Port 1	SDIN	SDIN	SCL	RFR	MOSI
Port 2	CLK	CLK	-	TX	CLK
Port 3	CS	CS	-	RX	CS
Port 4	-	D/C	-	-	CS1

QCC711 serial engine ports in Table 8-3 can be mapped to specific PIOs, see *Related Information*.

RELATED INFORMATION

"PIO" on page 40

8.4.1 UART

QCC711 has the following UART features:

- 3 x UARTs
- up to 2 Mbaud maximum UART rate capability
- hardware flow control
- programmable fractional baud rate generation from 32 MHz system clock
- DMA to and from system memory to reduce FIFO size and processor load
- 2 x UARTs supporting 9-bit data transfer mode

QCC711 has a standard UART serial interface that provides a simple mechanism to communicate with other serial devices using the RS232 protocol. The UART interface multiplexes with PIOs and other functions. Hardware flow control is optional. Table 8-4 lists possible UART settings.

Table 8-4 UART configuration options

Parameter		Possible value
Baud rate	Minimum	2400 (≤1%Error)
	Maximum	2 MBd (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd, or Even
Number of stop bits		1 or 2
Bits per byte (Applies to all Serial Engines)		8
Bits per byte (Applies to SE0 and SE1)		9

Table 8-5 lists supported baud rates and the QCC711 percentage error for that rate.

Table 8-5 Supported UART baud rates

Supported UART baud rate	Error (%) [a]
2400	0.04
4800	0.16
9600	0.16
19200	0.16
38400	0.16
115200	2.12
500000	0.00
1000000	0.00
2000000	0.00

[a] Error rates are based on internal divider clocks only and do not include XTAL error.

8.4.2 I²C interfaces

QCC711 has the following I²C features:

- 2 x I²C controller interfaces
- 1 x I²C peripheral interface
- 100 kbps, 400 kbps, and 1000 kbps rate
- external pull-up resistors required
- supports DMA to and from system memory to reduce FIFO size and processor load

8.4.3 3-wire SPI for display

Supported by:

- SE 0 on PIO[8:5]
- SE 1 on PIO[20:16]

8.4.4 4-wire SPI for display

Supported by:

- SE 0 on PIO[8:5]
- SE 1 on PIO[20:16]

8.4.5 True 4-wire SPI

QCC711 has the following SPI features:

- capable of concurrent operation, with DMA support
- clock divider for lower frequency operation with limited capability devices
- 4-wire 8-bit controller mode for external flash, other SPI-based displays/sensors, and standard peripherals
- 4-wire 8-bit SPI peripheral mode
- 32-bit mode with DMA - for arbitrary pattern generation from memory under application firmware control. Output of this SPI mode may be connected to FTC inputs for extra application flexibility to drive LED patterns

9 PIO

QCC711 has 26 PIO pads, that have extensive multiplexing capabilities to access numerous digital peripherals, see Table 9-1.

NOTE When designing a product using the SE port mappings in Table 8-2, all need simultaneous consideration, along with the physical PCB constraints, see *Related Information*.

Related Information

"QCC711 serial engines and supported interfaces" on page 37
"QCC711 PIO multiplexing functions" on page 40

9.1 QCC711 PIO multiplexing functions

QCC711 PIOs are directly controlled from the Application subsystem using registers or configuration. When multiplexing functions, using QCC711 PIOs, select an individual PIO function from each column in Table 9-1.

NOTE Until otherwise configured, all PIOs are set as a control status register (CSR) of the processor.

NOTE 3-wire and 4-wire SPI interfaces are limited on SE0 to PIO[8:5] and SE1 to PIO[20:16].

Table 9-1 QCC711 PIO multiplexing functions

PIO port	Lead number	Debug and test	Serial engine	QSPI and radio coexistence	I²C, FTC, LED, and analog
PIO[25]	24	-	se_0_port_4_copy4 se_1_port_4_copy4 se_2_port_4_copy4 se_3_port_4_copy4	mstr_pta_coex_confx	Analog led_white_copy4
PIO[24]	23	-	se_0_port_3_copy4 se_1_port_3_copy4 se_2_port_3_copy4 se_3_port_3_copy4	mstr_pta_coex_status	Analog led_green_copy4 i2c_scl_copy10
PIO[23]	22	-	se_0_port_2_copy4 se_1_port_2_copy4 se_2_port_2_copy4 se_3_port_2_copy4	mstr_pta_coex_active	Analog led_red_copy4 i2c_sda_copy10
PIO[22]	21	-	se_0_port_1_copy4 se_1_port_1_copy4 se_2_port_1_copy4 se_3_port_1_copy4	slv_pta_coex_confx	Analog led_blue_copy4 i2c_scl_copy9
PIO[21]	20	-	se_0_port_0_copy4 se_1_port_0_copy4 se_2_port_0_copy4 se_3_port_0_copy4	slv_pta_coex_status	ftc_in[3] led_white_copy7 i2c_sda_copy9
PIO[20]	19	appss_trace_data_3	se_0_port_4_copy3 se_1_port_4_copy3	slv_pta_coex_active	led_white_copy6 i2c_scl_copy8

Table 9-1 QCC711 PIO multiplexing functions (cont.)

PIO port	Lead number	Debug and test	Serial engine	QSPI and radio coexistence	I²C, FTC, LED, and analog
PIO[19]	18	appss_trace_data_2	se_0_port_3_copy3 se_1_port_3_copy3 se_2_port_4_copy3 se_3_port_4_copy3	-	ftc3_out[2] led_white_copy5 i2c_sda_copy8
PIO[18]	17	appss_trace_data_1	se_0_port_2_copy3 se_1_port_2_copy3 se_2_port_3_copy3 se_3_port_3_copy3	-	ftc3_out[1] led_white_copy3 i2c_scl_copy7
PIO[17]	16	appss_trace_data_0	se_0_port_1_copy3 se_1_port_1_copy3 se_2_port_2_copy3 se_3_port_2_copy3	-	ftc3_out[0] led_green_copy3 led_white_copy10 i2c_sda_copy7
PIO[16]	15	appss_trace_clk	se_0_port_0_copy3 se_1_port_0_copy3 se_2_port_1_copy3 se_3_port_1_copy3	qspi_io3_copy1	ftc_in[2] led_red_copy3 led_white_copy9 i2c_scl_copy6
PIO[15]	14	-	se_0_port_4_copy2 se_2_port_0_copy3 se_3_port_0_copy3	qspi_io2_copy1	ftc2_out[0] led_blue_copy3 led_white_copy8 i2c_sda_copy6
PIO[14]	12	-	se_0_port_3_copy2 se_1_port_4_copy2 se_2_port_4_copy2 se_3_port_4_copy2	qspi_csb_copy1	ftc2_out[2] i2c_scl_copy5
PIO[13]	11	test_lf	se_0_port_2_copy2 se_1_port_3_copy2 se_2_port_3_copy2 se_3_port_3_copy2	qspi_miso_copy1	ftc2_out[1] i2c_sda_copy5
PIO[12]	10	SWO	se_0_port_1_copy2 se_1_port_2_copy2 se_2_port_2_copy2 se_3_port_2_copy2	qspi_mosi_copy1	i2c_scl_copy4
PIO[11]	9	test_hf	se_0_port_0_copy2 se_1_port_1_copy2 se_2_port_1_copy2 se_3_port_1_copy2	qspi_clk_copy1	ftc_in[1] i2c_sda_copy4
PIO[10]	7	SWD_DIO[a]	se_1_port_0_copy2 se_2_port_0_copy2 se_3_port_0_copy2	-	-

Table 9-1 QCC711 PIO multiplexing functions (cont.)

PIO port	Lead number	Debug and test	Serial engine	QSPI and radio coexistence	I²C, FTC, LED, and analog
PIO[9]	6	SWD_CLK[a]	se_1_port_4_copy1 se_2_port_4_copy1 se_3_port_4_copy1	-	-
PIO[8]	47	-	se_0_port_4_copy1 se_1_port_3_copy1 se_2_port_3_copy1 se_3_port_3_copy1	-	-
PIO[7]	46	-	se_0_port_3_copy1 se_1_port_2_copy1 se_2_port_2_copy1 se_3_port_2_copy1	-	led_green_copy1 i2c_scl_copy3
PIO[6]	44	-	se_0_port_2_copy1 se_1_port_1_copy1 se_2_port_1_copy1 se_3_port_1_copy1	-	ftc_in[0] led_red_copy1 i2c_sda_copy3
PIO[5]	43	-	se_0_port_1_copy1 se_1_port_0_copy1 se_2_port_0_copy1 se_3_port_0_copy1	qspi_io3_copy0	ftc1_out[2] led_blue_copy1 i2c_scl_copy2
PIO[4]	42	-	se_0_port_0_copy1 se_1_port_4_copy0 se_2_port_4_copy0 se_3_port_4_copy0	qspi_io2_copy0	ftc1_out[1] led_white_copy1 i2c_sda_copy2
PIO[3]	41	-	se_0_port_3_copy0 se_1_port_3_copy0 se_2_port_3_copy0 se_3_port_3_copy0	qspi_csb_copy0	ftc1_out[0] led_white_copy0 i2c_scl_copy1
PIO[2]	40	-	se_0_port_2_copy0 se_1_port_2_copy0 se_2_port_2_copy0 se_3_port_2_copy0	qspi_miso_copy0	ftc0_out[2] led_green_copy0 i2c_sda_copy1
PIO[1]	39	-	se_0_port_1_copy0 se_1_port_1_copy0 se_2_port_1_copy0 se_3_port_1_copy0	qspi_mosi_copy0	ftc0_out[1] led_red_copy0 i2c_scl_copy0
PIO[0]	38	-	se_0_port_0_copy0 se_1_port_0_copy0 se_2_port_0_copy0 se_3_port_0_copy0	qspi_clk_copy0	ftc0_out[0] led_blue_copy0 i2c_sda_copy0

[a] If an application or product requires these PIOs for features other than debug, ensure there is sufficient delay so that after power up it is possible to attach a debugger and stop the processor. If application code instantly remaps these PIOs away from SWD it is not possible to use serial wire debug.

9.2 Multi-function pin

NOTE QCC711 will only support the following functionality at **Production Information** status.

QCC711 has an input-only MFP.

The MFP can also connect to a push-button and be configured using software to trigger different types of reset. The MFP can be configured to detect an edge, a short press, or a long press. The timing durations for the presses are not exact because they are estimations that use the internal slow clock.

10 Root-of-Trust subsystem

The QCC711 Root-of-Trust subsystem dedicated central processing unit (CPU) is designed to provide a segregated execution environment for the hardware acceleration of several security primitives and the provision of higher layer services.

Figure 10-1 shows the QCC711 Root-of-Trust subsystem.

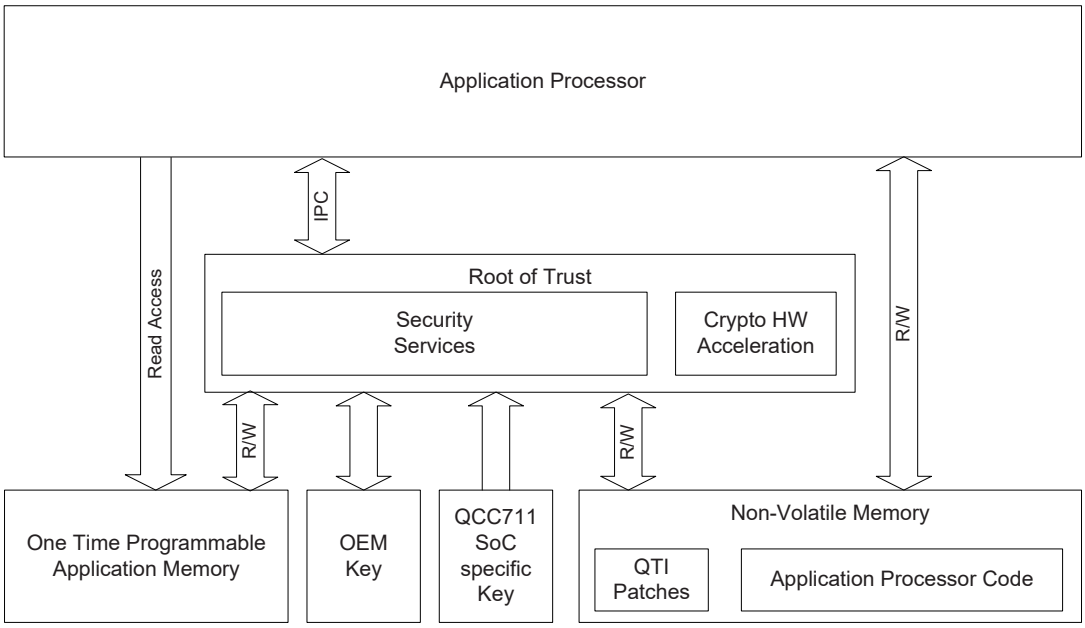

Figure 10-1 QCC711 Root-of-Trust subsystem

10.1 Security services

Using the provided application programming interface (API) over inter-processor communication (IPC), the QCC711 Root-of-Trust subsystem is designed to provide security services that include:

- "Secure boot (authentication at boot of Qualcomm Technologies Inc. (QTI) patches and optional authentication of the original equipment manufacturer (OEM) application)"
- "Secure debug (optional authenticated debug re-enablement)"
- Provisioning of one-time programmable (OTP) memory
- Higher layer security services, including:
  - "Secure provisioning of an OEM chosen key"
  - "Secure communication, using the OEM chosen key as root key for the derivation of OEM designed, use case specific keys"
  - "Secure provisioning of QTI patches and device application in NVM"
  - "Secure over-the-air (OTA) update of QTI patches and device application"
- Higher layer security services, including:
  - "Authenticated Management Operation"

- Leveraging a QTI authenticated and SoC specific key, services include:
  - "SoC Authentication"
  - "Remote attestation of the state of a device"
  - "Confidential Management Operation"
  - "Secure Onboarding of a device on an Internet of Things (IoT) network"

10.2 Security capabilities

QCC711 Root-of-Trust subsystem security capabilities include hardware acceleration of the algorithms listed in the Security section in *Related Information*.

RELATED INFORMATION

"QCC711 device details" on page 5

11 PMU subsystem

Figure 11-1 shows the QCC711 PMU subsystem.

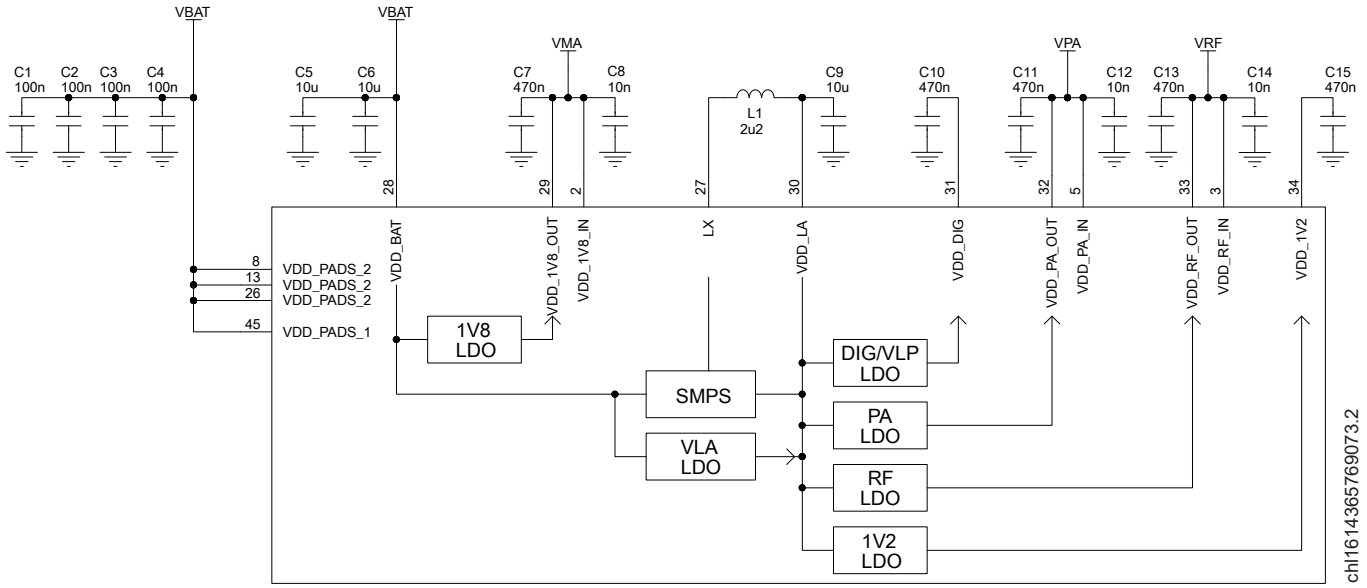

Figure 11-1 PMU subsystem

11.1 PMU subsystem features

The QCC711 PMU subsystem features:

- direct battery attachment to a 3 V coin cell
- an integrated PMU containing a switch-mode power supply (SMPS) and several low (voltage) drop-out (LDO)s:
  - 1.35 V supply by SMPS for good efficiency up to 93% that works in two modes:
    - pulse frequency modulation (PFM) mode during Active state up to 80 mA
    - ultra low power (ULP) mode during Sleep state up to 1 mA
  - LDOs / linear regulators generate other voltages for use on QCC711 (variable digital supply, 1.1 V, 1.15 V, 1.2 V, and 1.8 V)
- a temperature sensor to provide PMU temperature readings for customer applications
- battery voltage measurement
- battery brownout detector and display update comparators with programmable reference voltages
- on-chip resistance-capacitance (RC) oscillators for Sleep and Active states
- loads for battery resistance measurement
- RRAM power switch, with a power fail detect comparator
- light-dependent resistor (LDR) sensing functionality

11.2 10-bit SAR ADC

QCC711 has a 10-bit successive approximation register (SAR) analog-to-digital converter (ADC), that has an internal reference taken from VDD_1V8.

Two production calibration values are stored to compensate for gain and offset.

The ADC has a front-end multiplex enabling it to measure a range of signals in QCC711, and some external PIOs:

- Battery
- PIO[25:22]

RELATED INFORMATION

"QCC711 example application schematic" on page 49

11.3 Battery voltage sensor

Using the QCC711 internal ADC, battery voltage is measurable. An internal potential divider of 3, divides the voltage down to within the input range of the ADC.

11.4 Battery load cells

There are two, nominal 600 Ω, load cells that can be enabled to determine the impedance of a typical coin cell.

The delta change in current draw when adding a known load can be used to measure the internal resistance of an external battery.

Figure 11-2 shows battery resistance in QCC711.

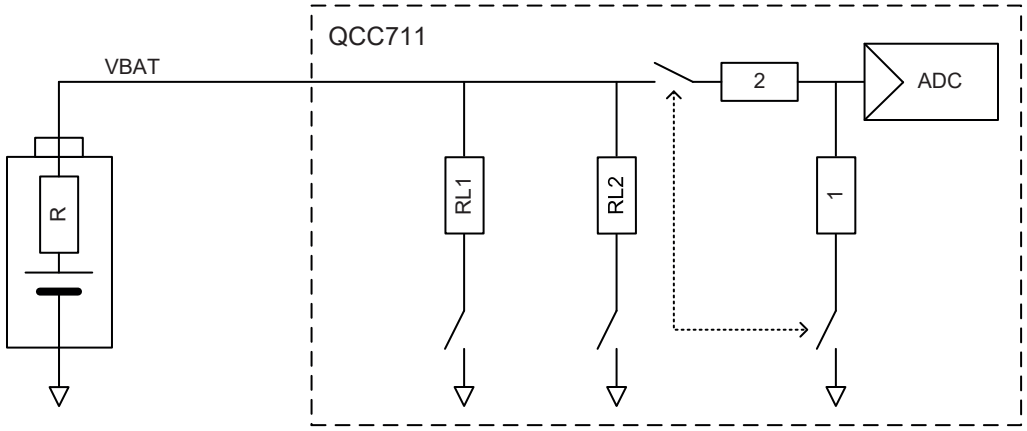

Figure 11-2 Battery resistance

NOTE There is a small increase in chip consumption as voltage decreases. This limits the ultimate accuracy that can be achieved. For small values of battery internal resistance, the estimation is poor. As the value becomes larger it may not be desirable to always load the cell with both of the load cells, because this would risk causing a brown out.

11.5 Analog inputs on PIO

To use QCC711 analog capability, a PIO pad has to be first set as an input, and have pull up and pull down disabled.

There are two modes:

- Default mode: inserts a divide-by-2 potential divider of nominal impedance of 180 kΩ - this ensures that whenever a signal is applied to the PIO (or if the pad is accidentally left output high or with the pull up) the operation of QCC711 is not compromised
- Direct mode: if the converted signal is both sensitive to the potential divider and under 1.8 V it is possible to bypass the divider, and connect directly to the ADC

11.6 Reading an LDR using a PIO

To read an LDR using a PIO, configure PIO[23] or PIO[22] to pull up to the VDD_1V8 net using an internal 100 kΩ resistor.

The ADC can then read the analog voltage of the PIO that is pulled down by the LDR component. The returned ADC reading allows the designer to ascertain the level of light exposed to the LDR.

11.7 PMU temperature sensor measurement accuracy

Measurement	Min	Typ	Max	Unit
PMU temperature sensor accuracy range 0°C ≤ T ≤ 50°C	-	-	2.0	°C
PMU temperature sensor accuracy range -30°C ≤ T < 0°C and 50°C < T ≤ 85°C	-	-	2.5	°C
Approximate temperature sensor step size (LSB)	-	0.33	-	°C
Temperature corrected resolution	-	0.01	-	°C

12 QCC711 example application schematic

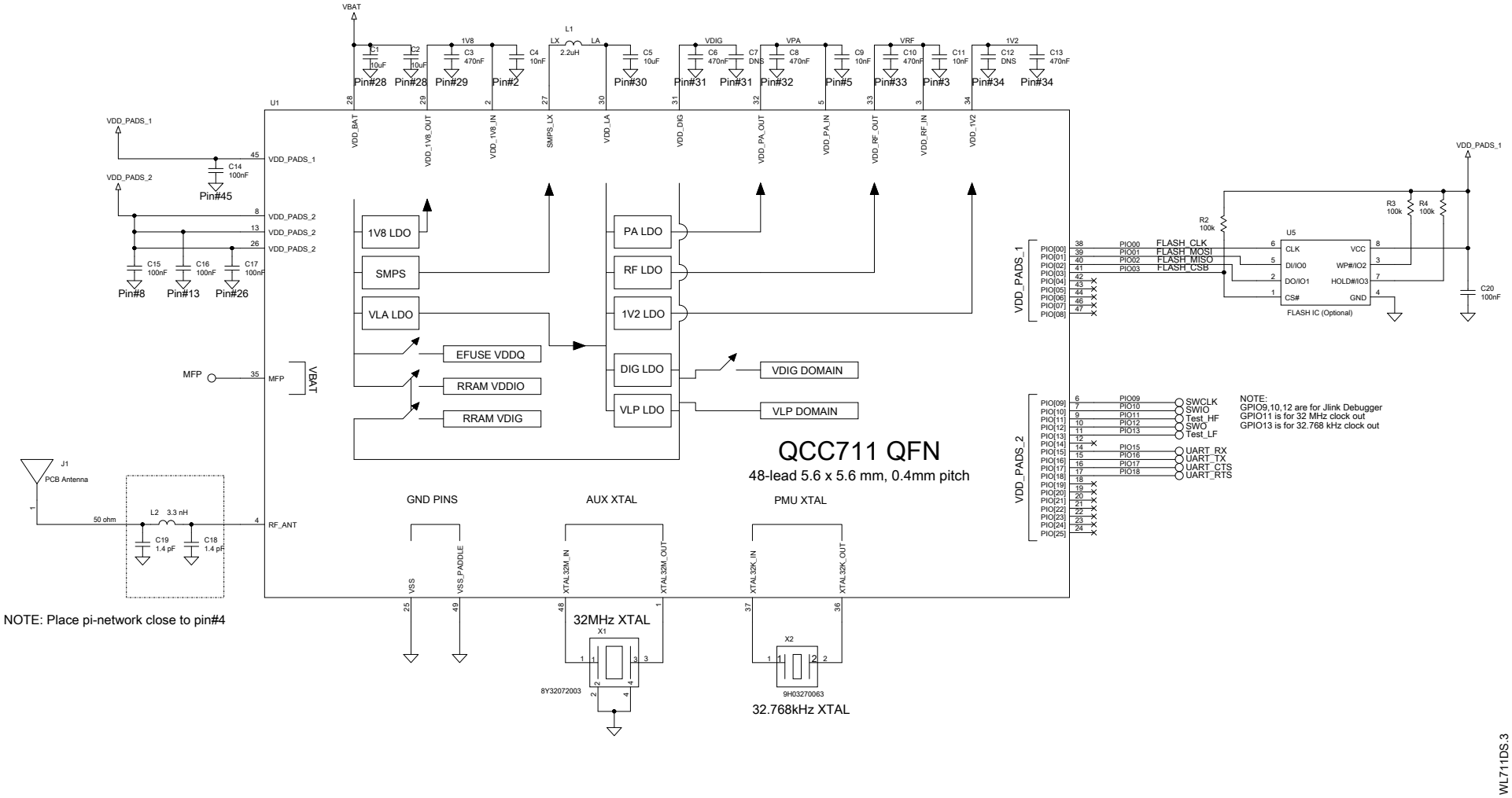

Figure 12-1 QCC711 example application schematic

13 Electrical characteristics

13.1 Absolute maximum ratings

Parameter	Pin	Min	Max	Unit
Battery voltage	VBAT	VDD_PADS_2	3.63	V
I/O Port 1 supply	VDD_PADS_1	VSS - 0.3	3.63	V
I/O Port 2 supply	VDD_PADS_2	VSS - 0.3	3.63	V
Digital I/O	PIO[25:9]	VSS - 0.3	VDD_PADS_2 + 0.3	V
	PIO[8:0]	VSS - 0.3	VDD_PADS_1 + 0.3	V
	MFP	VSS - 0.3	VBAT + 0.3	V
RF input	RF_ANT	-	-10	dBm
RF supply	RF_IN	RF_OUT	RF_OUT	V
PA supply	PA_IN	PA_OUT	PA_OUT	V
1.8 V supply	1V8_IN	1V8_OUT	1V8_OUT	V
1.2 V	XTAL_32K_IN	VSS - 0.3	VDD_1V2	V
	XTAL_32K_OUT	VSS - 0.3	VDD_1V2	V
1.8 V	XTAL_32M_IN	VSS - 0.3	VDD_1V2	V
	XTAL_32M_OUT	VSS - 0.3	VDD_1V2	V
All ground / VSS pads	-	0	0	V
Storage temperature	-	-40	85	°C

CAUTION Stressing the device beyond the Absolute Maximum Ratings may cause instantaneous and permanent damage.

Prolonged exposure beyond the Recommended Operating Conditions may permanently affect device reliability and/or performance. Device performance is not guaranteed beyond the Recommended Operating Conditions.

13.2 Recommended operating conditions

Parameter	Pin	Min	Max	Unit
Battery voltage	VBAT	1.71	3.6	V
I/O Port 1 supply	VDD_PADS_1	0	3.6	V
I/O Port 2 supply	VDD_PADS_2	0	3.6	V
Digital I/O	PIO[25:9]	VSS	VDD_PADS_2	V
	PIO[8:0]	VSS	VDD_PADS_1	V
	MFP	VSS	VBAT	V
RF supply	RF_IN	RF_OUT	RF_OUT	V
PA supply	PA_IN	PA_OUT	PA_OUT	V
1.8 V supply	1V8_IN	1V8_OUT	1V8_OUT	V
All ground / VSS pads	-	0	0	V
Operating temperature range	-	-40	85	°C

NOTE The following pins should have no voltage applied to them. Any voltage present is self-generated.

- RF_ANT
- XTAL_32K_IN
- XTAL_32K_OUT
- XTAL_32M_IN
- XTAL_32M_OUT
- All PMU output pins

13.3 SMPS

Parameter	Condition	Min	Typ	Max	Unit
Input supply	-		VBAT		-
DC output voltage	-		1.35		V
Output voltage accuracy	Including transients	-5	-	5	%
Output filter inductance	-	1.76[a]	2.2	2.64	µH
Inductor Saturation Current	-	-	-	500	mA
Inductor ESR (10 kHz – 1 MHz)	-	-	-	100	mΩ
Output filter capacitance	-	5	10	12	µF
Total capacitance on the SMPS output	-	5	10	12	µF
PFM mode[b]					
Output Current	-	-	-	80	mA
Peak Conversion efficiency	-	-	86	-	%
ULP mode	-				
Output Current	-	-	-	1	mA
Peak Conversion efficiency	-	-	86	-	%

[a] Including tolerances and derating
[b] ULP mode is used in sleep/storage modes

13.4 Digital terminals

Digital terminals	Min[a]	Typ	Max[a]	Unit
VIL input logic level low	VSS	VSS	0.3 * VDD	V
VIH input logic level high	0.7 * VDD	VDD	VDD	V
Drive current (configurable)	2	12	12	mA
VOL output logic level low, at max rated drive	VSS	-	0.8 * VDD	V
VOH output logic level high, at max rated drive	0.2 * VDD	-	VDD	V
Pull up[b]	17	21	49	kΩ
Pull down[b]	17	22	50	kΩ

[a] VDD is the respective VDD_PADS supply for the given PIO.
[b] Use of 10 k pull resistors on the PCB should be done with care, because this could result in a pad being held near mid-rail.

13.5 MFP terminals

Digital terminals	Min	Typ	Max	Unit
VIL input logic level low	VSS	VSS	0.3 * VBAT	V
VIH input logic level high	0.7 * VBAT	VBAT	VBAT	V
Pull down	3	5	7	MΩ

13.6 Analog terminals

Analog terminals[a]	Min	Typ	Max	Unit
VIL input logic level low	VSS	-	-	V
VIH input logic level high	-	-	VDD_PADS_2	V
VIH input logic level high (PMU divider in bypass)	-	-	VDD_1V8_OUT	V

[a] These values apply to PIO[25:22] when used. Before selecting analog capability, the digital feature of the respective PIO must be set to input with pulls disabled.

14 Bluetooth performance

NOTE For detailed QCC711 Bluetooth performance information, see *QCC71x Bluetooth Performance Specification* (80-WL710-72).

14.1 Bluetooth radio characteristics: Low Energy 1 Mb/s

Table 14-1 Bluetooth Low Energy 1 Mb/s transmitter performance at 25°C

RF characteristics, VBAT = 3.0 V		Notes	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Maximum RF transmit power		a	5	7	-	-20 to +10	dBm
In-band spurious emissions	$F = F_0 \pm 2$ MHz	b, c	-	-41	-20	≤-20	dBm
	$F > F_0 \pm 3$ MHz	b, c	-	-58	-30	≤-30	dBm
2nd harmonic content		d	-	-35	-	-	dBm
3rd harmonic content		d	-	-47	-	-	dBm

[a] Specified Min value is based on statistical variance and represents the absolute limit rather than expected performance.
[b] Measured at F_0 = 2440 MHz.
[c] Exceptions in up to three bands are allowed. For exceptions, $P_{TX} \leq$ -20 dBm.
[d] Conducted measurement at RF port. Use of an appropriate filter will attenuate transmit harmonics.

Table 14-2 Bluetooth Low Energy 1 Mb/s receiver performance at 25°C

RF characteristics, VBAT = 3.0 V	Frequency (GHz)	Notes	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Sensitivity at 30.8% PER	2.402	a	-	-96	-94	≤-70	dBm
	2.440	a	-	-96	-94		
	2.480	a	-	-96	-94		
Sensitivity at 30.8% PER (Boost Mode)	2.402	a	-	-99	-97	≤-70	dBm
	2.440	a	-	-99	-97		
	2.480	a	-	-98	-96		
Maximum received signal at 30.8% PER		b	-10	>-9	-	≥-10	dBm

[a] Measured using test packets with 37 octet payload.
[b] Measured in accordance with the RF-PHY/RCV-LE/CA/BV-07-C test. Random number of packets transmitted by tester of which 50 % have corrupted CRCs. Wanted signal level is -30 dBm.

14.2 Bluetooth radio characteristics: Low Energy 2 Mb/s

Table 14-3 Bluetooth Low Energy 2 Mb/s transmitter performance at 25°C

RF characteristics, VBAT = 3.0 V		Notes	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Maximum RF transmit power		a	5	7	-	-20 to +10	dBm
In-band spurious emissions	$F = F_0 \pm 4$ MHz	b, c	-	-50	-20	≤-20	dBm
	$F = F_0 \pm 5$ MHz	b, c	-	-53	-20	≤-20	dBm
	$F > F_0 \pm 6$ MHz	b, c	-	-59	-30	≤-30	dBm
2nd harmonic content		d	-	-35	-	-	dBm
3rd harmonic content		d	-	-48	-	-	dBm

[a] Specified Min value is based on statistical variance and represents the absolute limit rather than expected performance.
[b] Measured at F_0 = 2440 MHz.
[c] Exceptions in up to three bands are allowed. For exceptions, $P_{TX} \leq$ -20 dBm.
[d] Conducted measurement at RF port. Use of an appropriate filter will attenuate transmit harmonics.

Table 14-4 Bluetooth Low Energy 2 Mb/s receiver performance at 25°C

RF characteristics, VBAT = 3.0 V	Frequency (GHz)	Notes	Min	Typ	Max	Bluetooth v5.4 specification	Unit
Sensitivity at 30.8% PER	2.402	a	-	-91	-89	≤-70	dBm
	2.440	a	-	-92	-90		
	2.480	a	-	-91	-89		
Sensitivity at 30.8% PER (Boost Mode)	2.402	a	-	-95	-93	≤-70	dBm
	2.440	a	-	-95	-93		
	2.480	a	-	-94	-92		
Maximum received signal at 30.8% PER		b	-10	>-9	-	≥-10	dBm

[a] Measured using test packets with 37 octet payload.
[b] Measured in accordance with the RF-PHY/RCV-LE/CA/BV-07-C test. Random number of packets transmitted by tester of which 50 % have corrupted CRCs. Wanted signal level is -30 dBm.

15 Power consumption

NOTE Power consumption values listed are taken from the demo application in the QCC711 SDK.

Typical measurement conditions unless stated otherwise are:

- Supply voltage 3.0 V, applied to VBAT, VDD_PADS1, and VDD_PADS2
- Test temperature 25 °C

15.1 Transmitter power consumption

Table 15-1 Transmitter power consumption

Radio	Conditions	MCU state	dBm	Average current	Unit
Tx	Modem current included.	Active[a]	0	9.9	mA
Tx	Modem current included.	Active[a]	4	13.6	mA
Tx	Modem current included.	Active[a]	7	16.9	mA

[a] Applications subsystem (APSS) MCU and RoT MCU in shutdown.

15.2 Receiver power consumption

Table 15-2 Receiver power consumption

Radio	Conditions	MCU state	dBm	Average current	Unit
Rx Normal	Modem current included.	Active[a]	-95	4.5	mA
Rx Boost	Modem current included.	Active[a]	-98	4.6	mA

[a] APSS MCU and RoT MCU in shutdown.

15.3 Sleep and Hibernate state power consumption

Table 15-3 Sleep and Hibernate state power consumption

MCU state	Conditions	Average current	Unit
Sleep	Software controlled. 16 KB SRAM retained. 32 kHz crystal running.	1.5	µA
Hibernate	Software controlled. No SRAM retained. Internal LFLPO running.[a]	1.3	µA

[a] APSS MCU, Bluetooth subsystem (BTSS) MCU, and RoT MCU in shutdown.

16 RoHS compliance

This device meets the substance restriction requirement of the EU RoHS directive.

For further information, refer to the *Product Material Declaration* (PMD) for this device in CreatePoint.

17 Software development and tools

For information about QCC711 software development and tools, see *QCC711 Software Programming Guide* (80-61032-1).

18 Carrier, storage, and handling information

Carrier, storage, and handling information describes how to safely transport QCC711 devices.

18.1 Carrier

The QCC711 carrier system is tape and reel.

18.1.1 Tape and reel information

All QTIL tape carrier systems conform to EIA-481 standards.

Figure 18-1 and Table 18-1 show and list part orientation, maximum number of devices per reel, and dimensions for the QCC711 tape carrier.

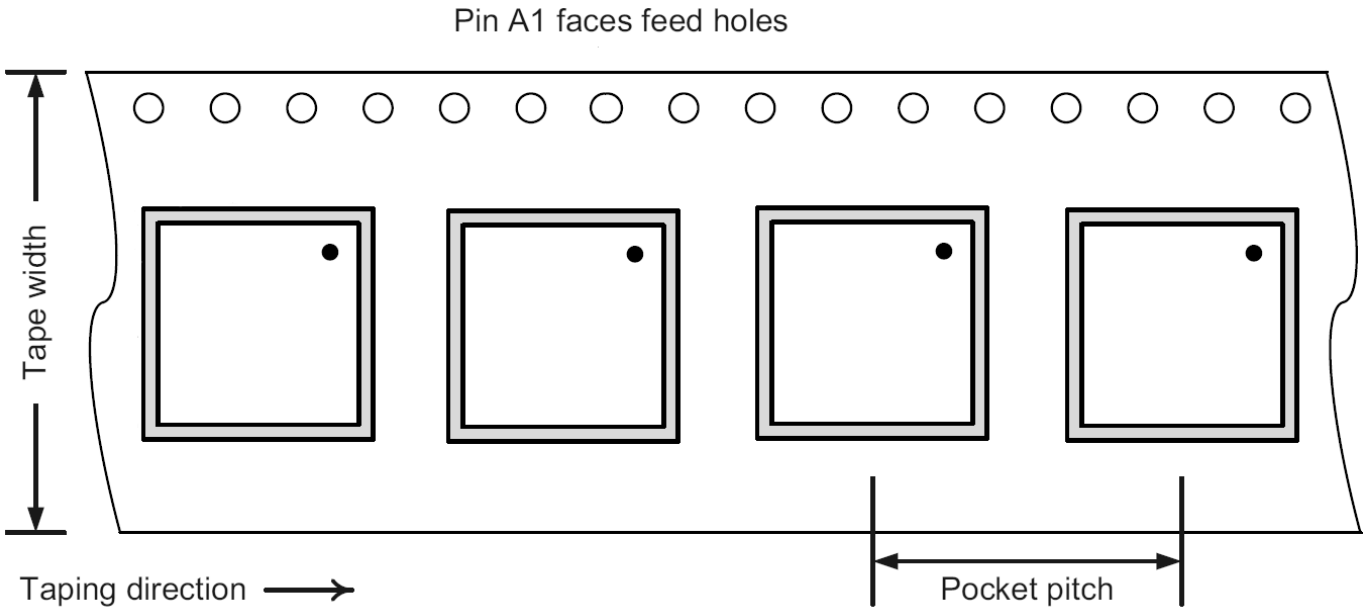

Figure 18-1 QCC711 carrier tape and part orientation

Table 18-1 QCC711 carrier tape dimensions

Tape feed:	Single	**Reel diameter:**	330 mm	**Tape width:**	16 mm
Units per reel:	4000	**Hub diameter:**	178 mm	**Pocket pitch:**	8 mm

Figure 18-2 shows recommendations for tape handling.

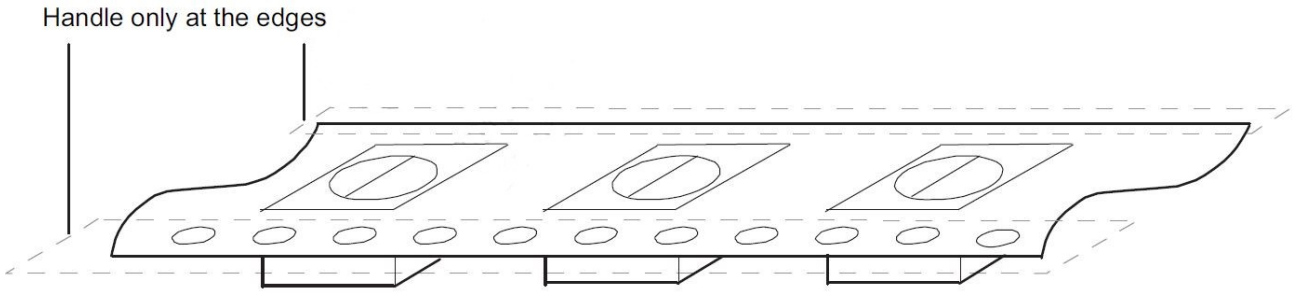

Figure 18-2 Tape handling recommendations

18.2 Storage

QCC711 device storage includes:

- Bagged storage conditions
- Out-of-bag duration

18.2.1 Bagged storage conditions

QCC711 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. For expected shelf life, see *IC Products Packing Method* (80-VK055-1).

18.2.2 Out-of-bag duration

Out-of-bag duration is the time a device can be on the factory floor before installation onto a PCB. It is defined by the device moisture sensitivity level (MSL) rating, see *Related Information*.

18.3 Handling

QCC711 device handling includes:

- Baking
- Electrostatic discharge

18.3.1 Baking

QCC711 devices require baking if storage conditions are exceeded. QCC711 devices do not require baking if storage conditions are not exceeded. Baking conditions are specified on the moisture-sensitive caution label attached to each bag. For details, see *IC Products Packing Method* (80-VK055-1).

CAUTION If baking is required, QCC711 devices must be transferred into trays that can be baked to at least 125°C. QCC711 devices should not be baked in tape and reel carriers at any temperature.

18.3.2 Electrostatic discharge

An electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTIL recommends implementing ESD control program such as ANSI/ESD S20.20-2014 or IEC 61340-5 (required for electronics manufacturing environment) to safely handle ESD sensitive products.

For QCC711 ESD ratings, see *Related Information*.

Related Information

"Part reliability" on page 62

18.4 Bar code label and packing for shipment

For all packing-related information, including bar code label details, see *IC Products Packing Method* (80-VK055-1).

19 Part reliability

Part reliability information for QCC-711-1-MQFN48C-TR-02-1 (v2.0) and QCC-711-1-MQFN48C-TR-03-1 (v2.1) includes:

- Silicon reliability results
- Package reliability results

19.1 Silicon reliability results

Table 19-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108F (Total samples from three different wafer lots)	240	Pass < 1000 DPPM[a]
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108F (Total samples from three different wafer lots)	239	Pass < 50 FIT
ESD – human-body model (HBM) rating JS-001-2017 (Total samples from one wafer lot)	3	(Lead 35 - MFP) Pass ±1.75 kV (All other leads) Pass ±2 kV
ESD – charged-device model (CDM) rating JS-002-2018 (Total samples from one wafer lot)	3	Pass ±500 V
Latch-up (I-test): EIA/JESD78D Trigger current: ±100 mA; temperature: 85 °C (Total samples from one wafer lot)	6	Pass
Latch-up (V-supply overvoltage): EIA/JESD78D Trigger voltage: Each VDD pin, stress at 1.5 × V_{ddmax} per device specification; temperature: 85 °C (Total samples from one wafer lot)	6	Pass

[a] Data is leveraged from other previously qualified product from TSMC 40 nm ULP process node and similar product family.

19.2 Package reliability results

Table 19-2 Package reliability results

Tests, standards, and conditions	Sample size	Result		
		AST	ASC	SPIL
Moisture resistance test (MRT): J-STD-020E Reflow at 260 +0/-5 °C (Total samples from three different assembly lots)	1386	Pass	Pass	Pass
Temperature cycle: JESD22-A104F Temperature: -55 °C to 125 °C; number of cycles: 500 Soak time at minimum/maximum temperature: 5 to 7 minutes Cycle rate: 2 cycles per hour (cph) Preconditioning: JESD22-A113-I MSL 3, reflow temperature: 260 +0/-5 °C (Total samples from three different assembly lots)	462	Pass	Pass	Pass
Unbiased highly accelerated stress test: JESD22-A118B 130 °C / 85 % RH and 96-hour duration Preconditioning: JESD22-A113G MSL 1, reflow temperature: 260 +0/-5 °C (Total samples from three different assembly lots)	462	Pass	Pass	Pass
Biased highly accelerated stress test: JESD22-A110E 110 °C / 85 % RH and 264-hour duration Preconditioning: JESD22-A113G MSL 3, reflow temperature: 260 +0/-5 °C (Total samples from three different assembly lots)	231	Pass	Pass	Pass
High-temperature storage life: JESD22-A103E Temperature 150 °C, 1000 hours (Total samples from three different assembly lots)	462	Pass	Pass	Pass

Document references

Document	Reference, date
Bluetooth Core Specification	Bluetooth Specification Version 5.4, 31 January 2023
IC Products Packing Method	80-VK055-1
QCC71x Bluetooth Performance Specification	80-WL710-72
QCC711 Hardware Design Guide	80-WL711-5
QCC711 Bluetooth Low Energy Device Revision Guide	80-WL711-4
QCC711 Software Programming Guide	80-61032-1
Typical Solder Reflow Profile for Lead-free Devices Information Note	80-CT462-1

Glossary

Term	Definition
ADC	Analog-to-digital converter
AES	Advanced encryption standard
AON	Always ON
API	Application programming interface
Arm	Arm Ltd.
Balun	Balanced/unbalanced interface or device that changes a balanced output to an unbalanced input or vice versa
Bluetooth	Set of technologies providing audio and data transfer over short-range radio connections
CPU	Central processing unit
CSR	Control status register
dBm	Decibels relative to 1 mW
DC	Direct current
DMA	Direct memory access
EIA	Electronic Industries Alliance
ELFR	Early life failure rate
ESD	Electrostatic discharge
ESL	Electronic shelf label
ESR	Equivalent series resistance
FIFO	First-in first-out (queue)
FSM	Finite state machine
FTC	Flexible timer/counter
GCC	Global clock controller
HCI	Host controller interface
HFLPO	High frequency low-power oscillator
HTOL	High temperature operating life
I/O	Input/output
IC	Integrated circuit
IoT	Internet of Things
IP	Intellectual property
IPC	Institute of Printed Circuits, see www.ipc.org
IPC	Inter-processor communication
I²C	Inter-integrated circuit interface

Term	Definition
KB	Kilobyte
kpcs	Thousand pieces
LDO	Low (voltage) drop-out
LDR	Light-dependent resistor
LED	Light-emitting diode
LFLPO	Low frequency low-power oscillator
LSB	Least significant bit (or byte)
Mbps	Megabits per second
MFP	Multi-function pin
MSL	Moisture sensitivity level
NFC	Near field communication
NSMD	Nonsolder mask defined
NVM	Non-volatile memory
OEM	Original equipment manufacturer
OTA	Over-the-air
OTP	One-time programmable
PCB	Printed circuit board
PFM	Pulse frequency modulation
PIO	Programmable input/output, also known as general-purpose I/O
PKA	Public-key authentication
PME	Power management engine
PMU	Power management unit
POR	Power on reset
PRNG	Pseudorandom number generator
PWM	Pulse width modulation
QFN	Quad-flat no-lead
QSPI	Quad serial peripheral interface (flash)
QTI	Qualcomm Technologies Inc.
QTIL	Qualcomm Technologies International, Ltd.
QUP	Qualcomm universal peripheral
RC	Resistance-capacitance (Oscillator)
RF	Radio frequency
RISC	Reduced instruction set computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/ EC)
ROM	Read only memory

Term	Definition
RoT	Root of Trust
RRAM	Resistive random-access memory
RTOS	Real-time operating system
Rx	Receive or receiver
SAR	Successive approximation register (ADC)
SE	Serial engine
SHA	Secure hash algorithm
SMPS	Switch-mode power supply
SoC	System on-chip
SPI	Serial peripheral interface
SRAM	Static random access memory
SWD	Serial wire debug
SWO	Single wire output
TLMM	Top-level mode multiplexing
Tx	Transmit or transmitter
UART	Universal asynchronous receiver transmitter
ULP	Ultra low power
Wi-Fi®	Wireless fidelity (IEEE 802.11 wireless networking)

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