Qualcomm Technologies, Inc.

# QCC74x Hardware Overview

80-WL740-11 Rev. AD

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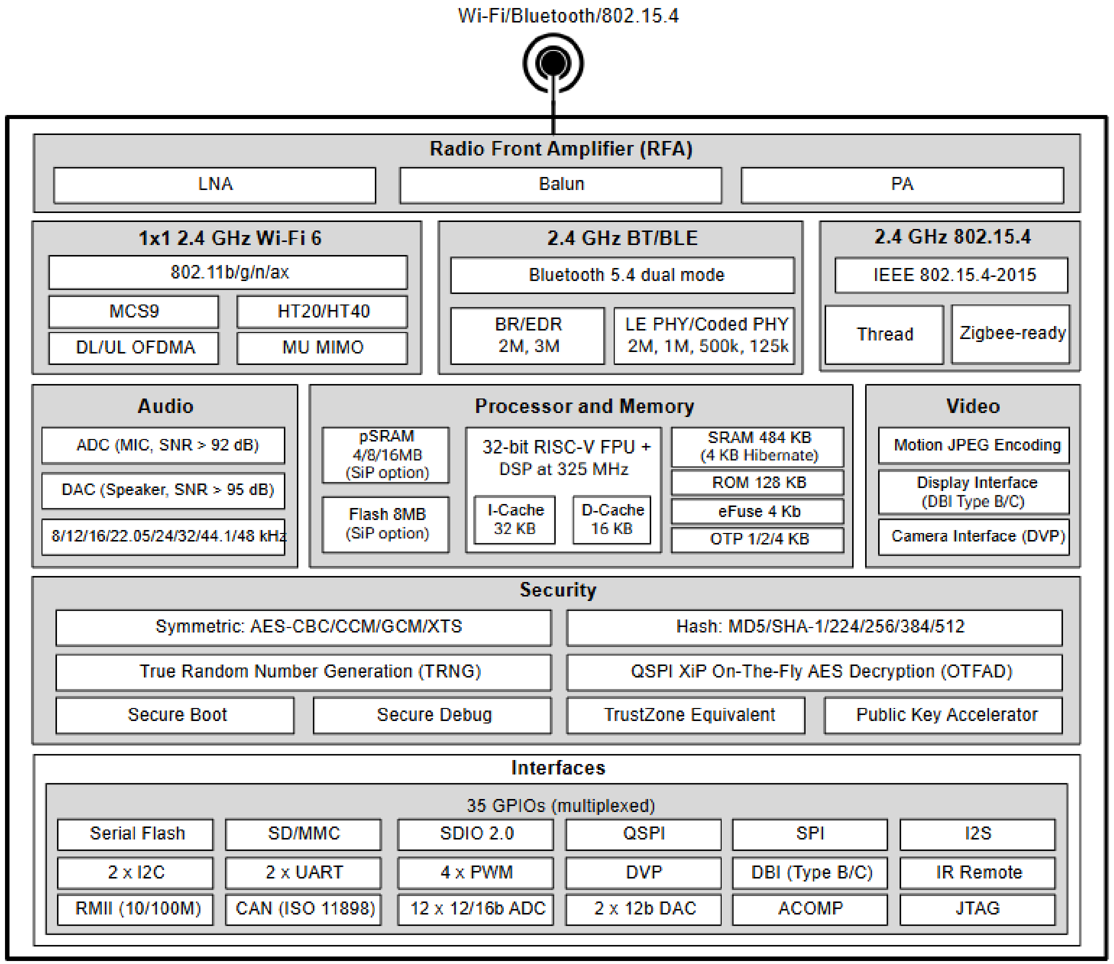
# Contents

Section 1

# QCC74x Chipset Overview

# QCC743/QCC744 Functional Block




Processor:

- 32-bit RISC-V at 325 MHz with DSP and FPU
- 128 KB ROM, 4 Kb eFuse and 1/2/4 KB OTP
- 484 KB on-chip SRAM (32 KB I-Cache and 16 KB D-Cache)
- Optional 4 MB (QCC744-2/4)/8 MB (QCC744-3)/16 MB (QCC744-5) pSRAM SiP
- Optional 8 MB (QCC744-4) NOR flash

Wireless connectivity:

- 1x1 2.4 GHz 802.11b/g/n/ax (Wi-Fi 6), HT20/HT40, MCS9
- Bluetooth 5.4 dual mode
- 802.15.4 (Thread and Zigbee-ready)

Advanced hardware security:

- Integrated hardware crypto acceleration
- Security services (secure boot, secure debug)
- PSA Certified Level 1

Peripherals:

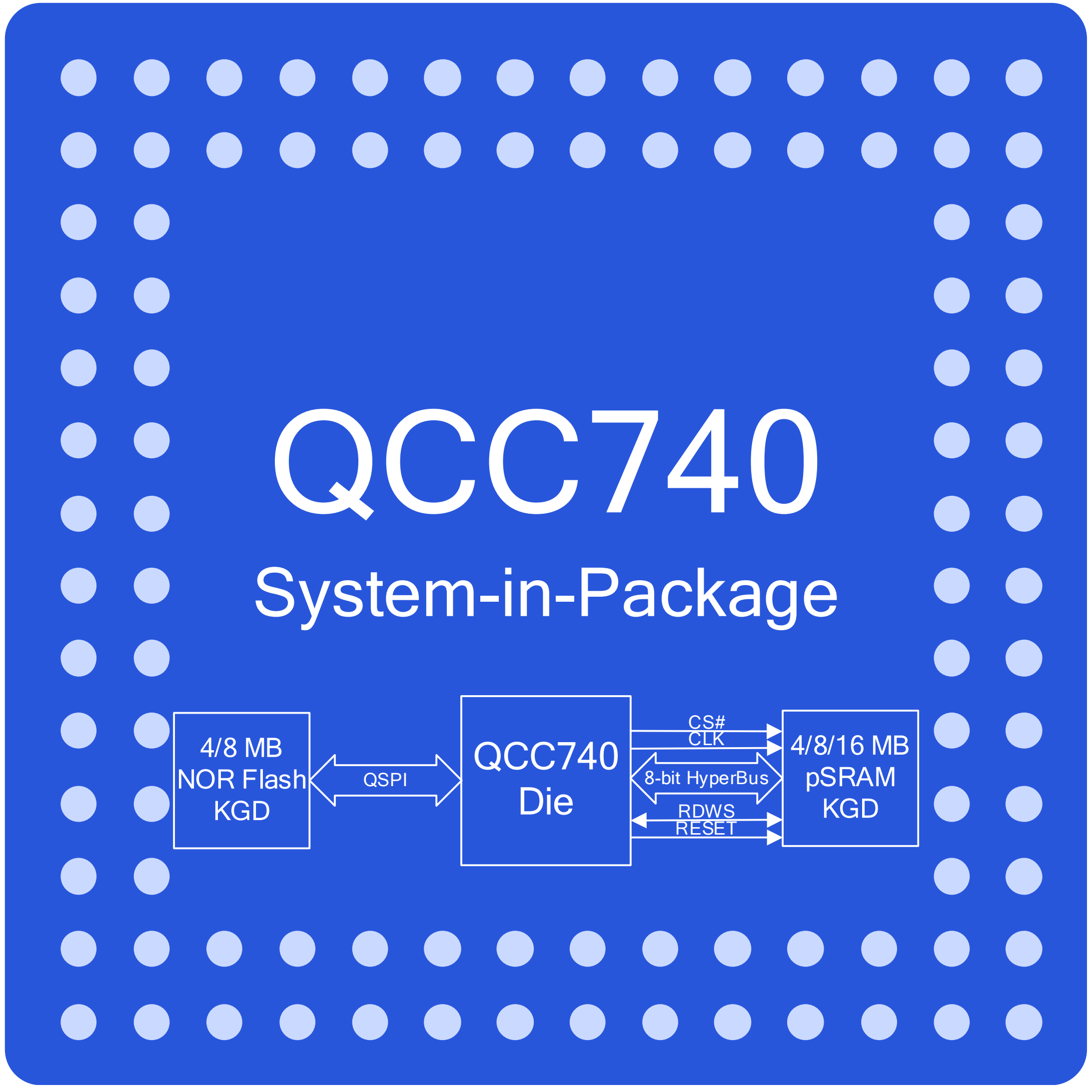
- Up to 35 GPIOs (multiplexed)
- SD/MMC/SF, SDIO, QSPI, SPI, I2C, I2S, UART, PWM, ADC/DAC, CAN (ISO 11898), RMII

Multimedia:

- Motion JPEG at 720p (15-25 fps), DVP, MIPI DBI
- 1-channel ADC and 1-channel DAC at 8 k to 96 k sampling rate

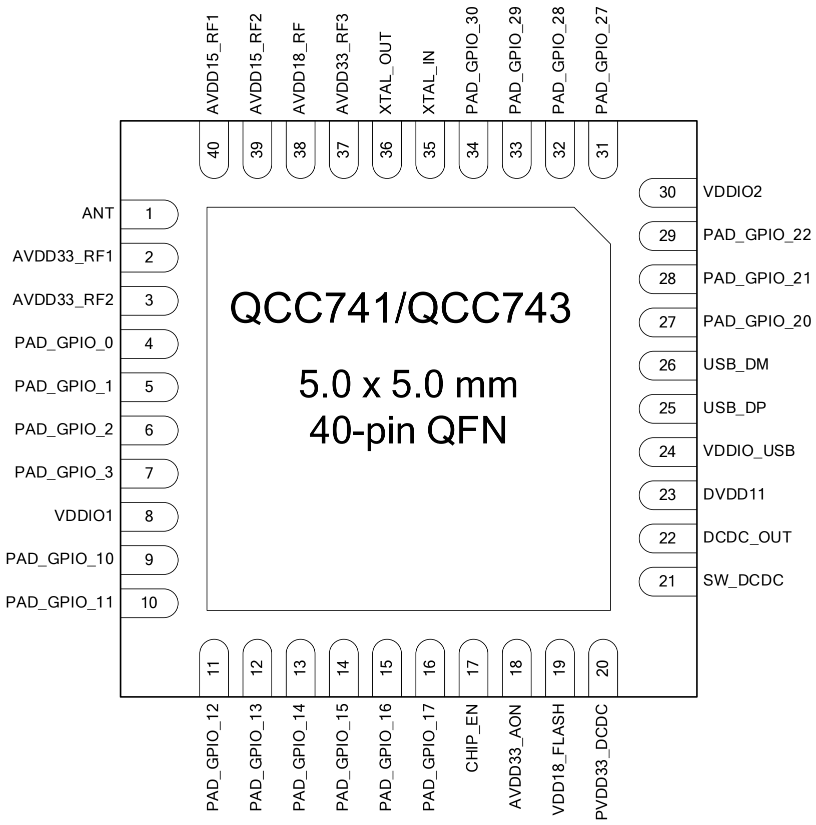
* USB will be supported in future chip spin.

# Optional Stacked Memory System-in-Package (SiP) (SRAM and NOR Flash)

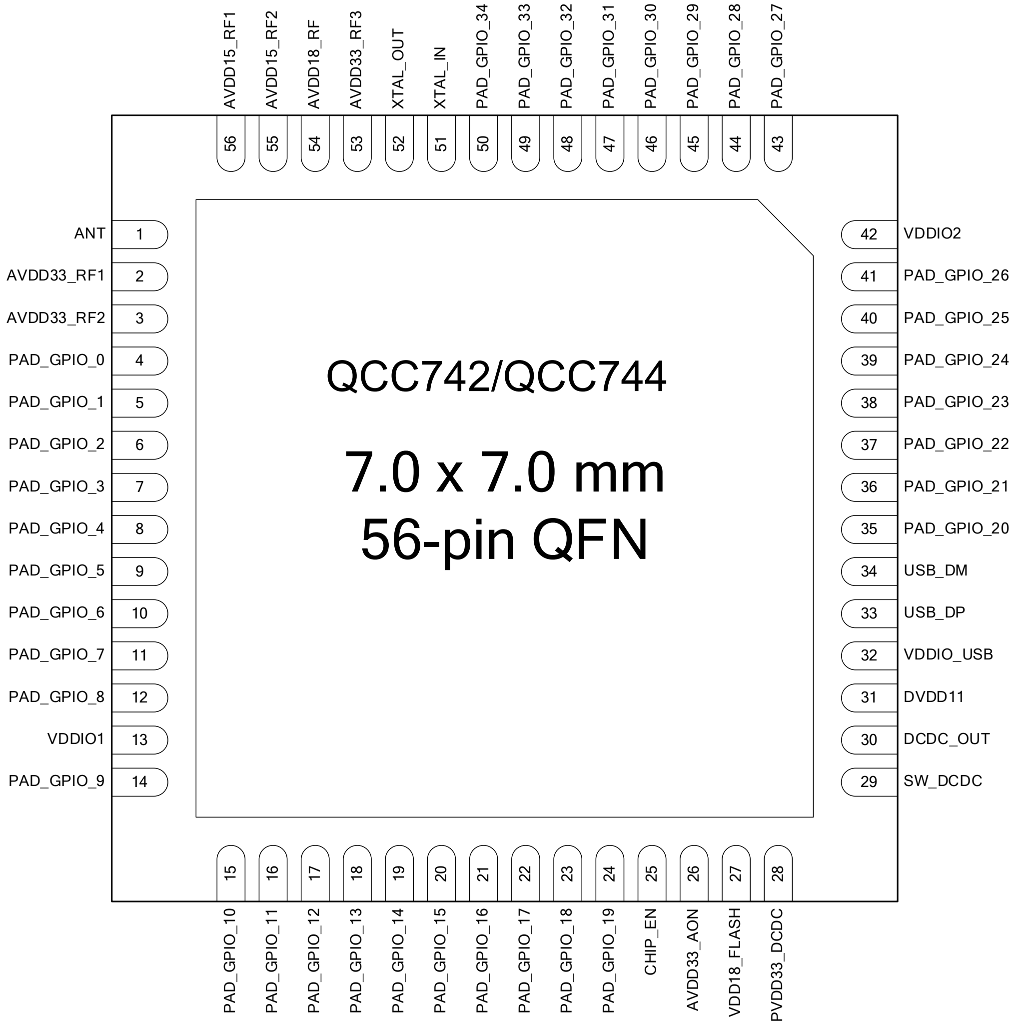


# QCC74x Package

QFN-40, 5.0 x 5.0 x 0.85 mm, 0.4 mm pitch




QFN-56, 7.0 x 7.0 x 0.85 mm, 0.4 mm pitch



Section 2

# QCC74x Features

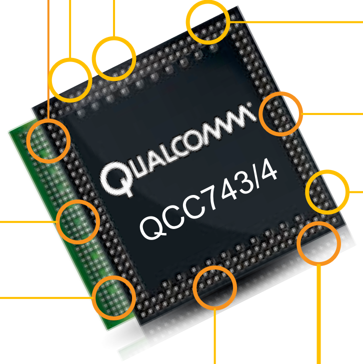
# QCC743/QCC744 Features

## Wi-Fi 6 + Bluetooth 5.4

**Hostless Architecture**
- 32-bit RISC-V @325MHz
- 128KB ROM
- 484KB SRAM

**Advanced Security**
- Integrated hardware crypto acceleration
- Security services (secure boot, secure debug)
- PSA Certified Level 1

**Multi-connectivity**
- Smart coex and concurrency mgmt to maximize coverage
- Concurrent BLE/802.15.4/Wi-Fi Operations




**BLE**
- Low Energy and Mesh

**Wi-Fi**
- 2.4 GHz 11ax

**15.4**
- Thread and Zigbee-ready

**Multiple protocols**
- Thread
- ZigBee-ready
- Matter

**Full Network Stack**
- Concurrent Modes
- TCP/IP, HTTP Server/Client
- IPv4/IPv6 networking

**XIP**
- Executing code in place from an external flash

**Wide range of peripherals**
- SPI, GPIO, I2C, I2S, UART
- SDIO, USB2.0
- PWM, 12-bit ADC, 12-bit DAC,
- IR remote, RMII (10/100 Ethernet)
- CAN (ISO 11898)

**Low power consumption**
- Various power modes
- Low power consumption

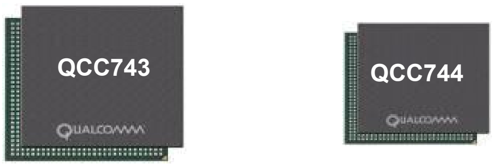
* USB will be supported in future chip spin.

# QCC743/QCC744 Features (cont.)

32-bit RISC-V processor with an FPU and DSP running up to 325 MHz + CNSS + 1x1 Wi-Fi 6, Bluetooth 5.4 qualifications, and IEEE 802.15.4 (Thread and Zigbee-ready).

Features and packages:

- QCC743/QCC744 are Wi-Fi 6 + Bluetooth 5.4 + 802.15.4 (Thread and Zigbee-ready) combo chipsets for ultra low-power applications. QCC743/QCC744 include two subsystems: wireless and microcontroller.
  - The wireless subsystem contains 2.4 GHz radio, Wi-Fi 802.11b/g/n/ax, Bluetooth/Bluetooth Low Energy, and IEEE802.15.4 baseband/MAC designs.
  - The microcontroller subsystem contains a low-power 32-bit RISC-V CPU with floating point units, DSP units, high-speed cache, and memories. The embedded Power Management Unit (PMU) controls the low-power modes. The microcontroller also supports various security features.
- QCC743/QCC744 support SDU, SD/MMC (SDH), SPI, UART, I2C, I2S, PWM, GPDAC, GPADC, ACOMP, and GPIOs interfaces. QCC744 supports additional interfaces for camera, display, MJPEG, audio codec, and Ethernet.
- QCC743 supports 19 GPIOs.
- QCC744 supports 35 GPIOs.




*QCC744 has more scalable GPIOs than QCC743.*

# QCC743/QCC744 Series Product SKU Released

**Mass Production**

| Device | Configuration | Stacked Memory | | Grade | Package | Revision |
|---|---|---|---|---|---|---|
| | | pSRAM | Flash | | | |
| QCC743-1 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 + 802.15.4 | - | - | -40°C – 105°C | QFN-40, 5 x 5 x 0.9 mm, 0.4 mm pitch | A1 |
| QCC744-2 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 + 802.15.4 | 4MB | - | -40°C – 85°C | QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch | A1 |

**Order Information**

| Device | Order Number | Grade | Packaging | Revision |
|---|---|---|---|---|
| QCC743-1 | QCC-743-1-MQFN40-MT-00-0 | -40°C – 105°C | Bulk | CS |
| | QCC-743-1-MQFN40-TR-00-0 | -40°C – 105°C | Reel | |
| QCC744-2 | QCC-744-2-MQFN56-MT-00-0 | -40°C – 85°C | Bulk | CS |
| | QCC-744-2-MQFN56-TR-00-0 | -40°C – 85°C | Reel | |

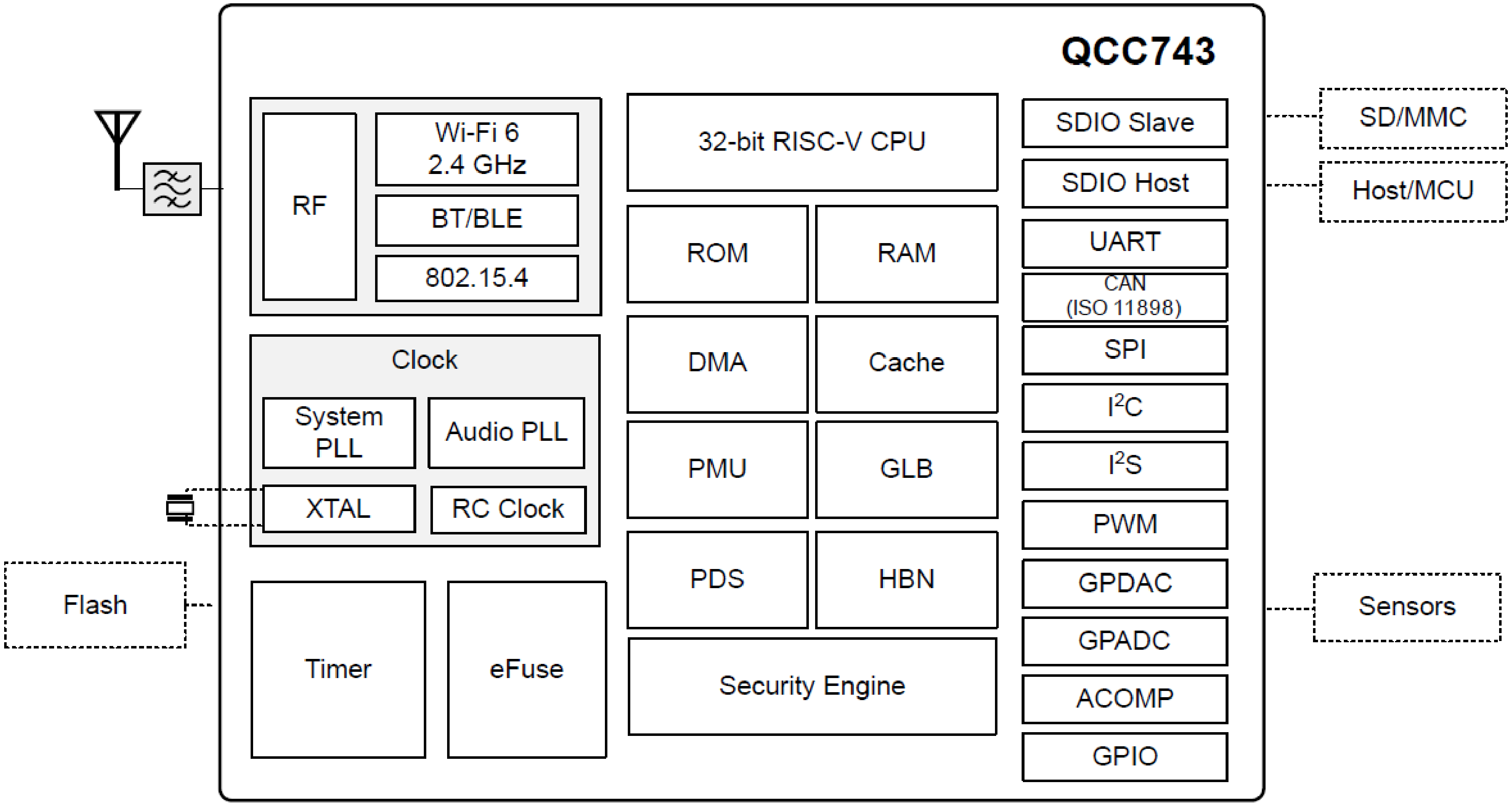
# QCC74x Series Product SKU Planned

| Device | Configuration | Stacked Memory | | Grade | Package | Status |
|---|---|---|---|---|---|---|
| | | pSRAM | Flash | | | |
| QCC741-1 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 | - | - | -40°C – 105°C | QFN-40, 5 x 5 x 0.9 mm, 0.4 mm pitch | Under Plan |
| QCC742-1 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 | - | - | -40°C – 105°C | QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch | Under Plan |
| QCC742-2 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 | 4MB | - | -40°C – 85°C | QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch | Under Plan |
| QCC742-3 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 | 8MB | - | -40°C – 85°C | QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch | Under Plan |
| QCC742-4 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 | 4MB | 8MB | -40°C – 85°C | QFN-56, 7 x 7 x 0.95 mm, 0.4 mm pitch | Under Plan |
| QCC742-5 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 | 16MB | - | -40°C – 85°C | QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch | Under Plan |
| QCC743-1 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 + 802.15.4 | - | - | -40°C – 105°C | QFN-40, 5 x 5 x 0.9 mm, 0.4 mm pitch | Released |
| QCC744-1 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 + 802.15.4 | - | - | -40°C – 105°C | QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch | Under Validation |
| QCC744-2 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 + 802.15.4 | 4MB | - | -40°C – 85°C | QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch | Released |
| QCC744-3 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 + 802.15.4 | 8MB | - | -40°C – 85°C | QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch | Under Plan |
| QCC744-4 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 + 802.15.4 | 4MB | 8MB | -40°C – 85°C | QFN-56, 7 x 7 x 0.95 mm, 0.4 mm pitch | Under Plan |
| QCC744-5 | 2.4 GHz 1x1 Wi-Fi 6 + Bluetooth 5.4 + 802.15.4 | 16MB | - | -40°C – 85°C | QFN-56, 7 x 7 x 0.9 mm, 0.4 mm pitch | Under Plan |

Section 3

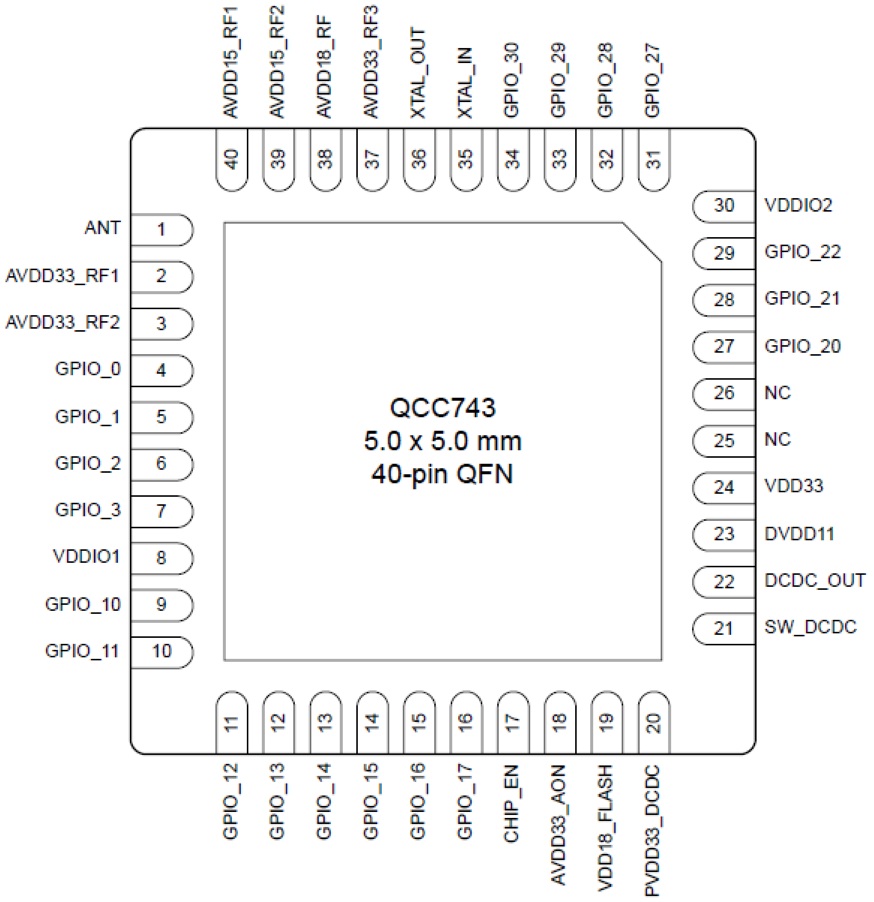
# QCC743 Introduction

# QCC743 Functional Block Diagram



# QCC743 Pin Map

QCC743 40-pin package includes 15 fixed power ports, 4 fixed analog ports, and up to 19 configurable GPIO ports.



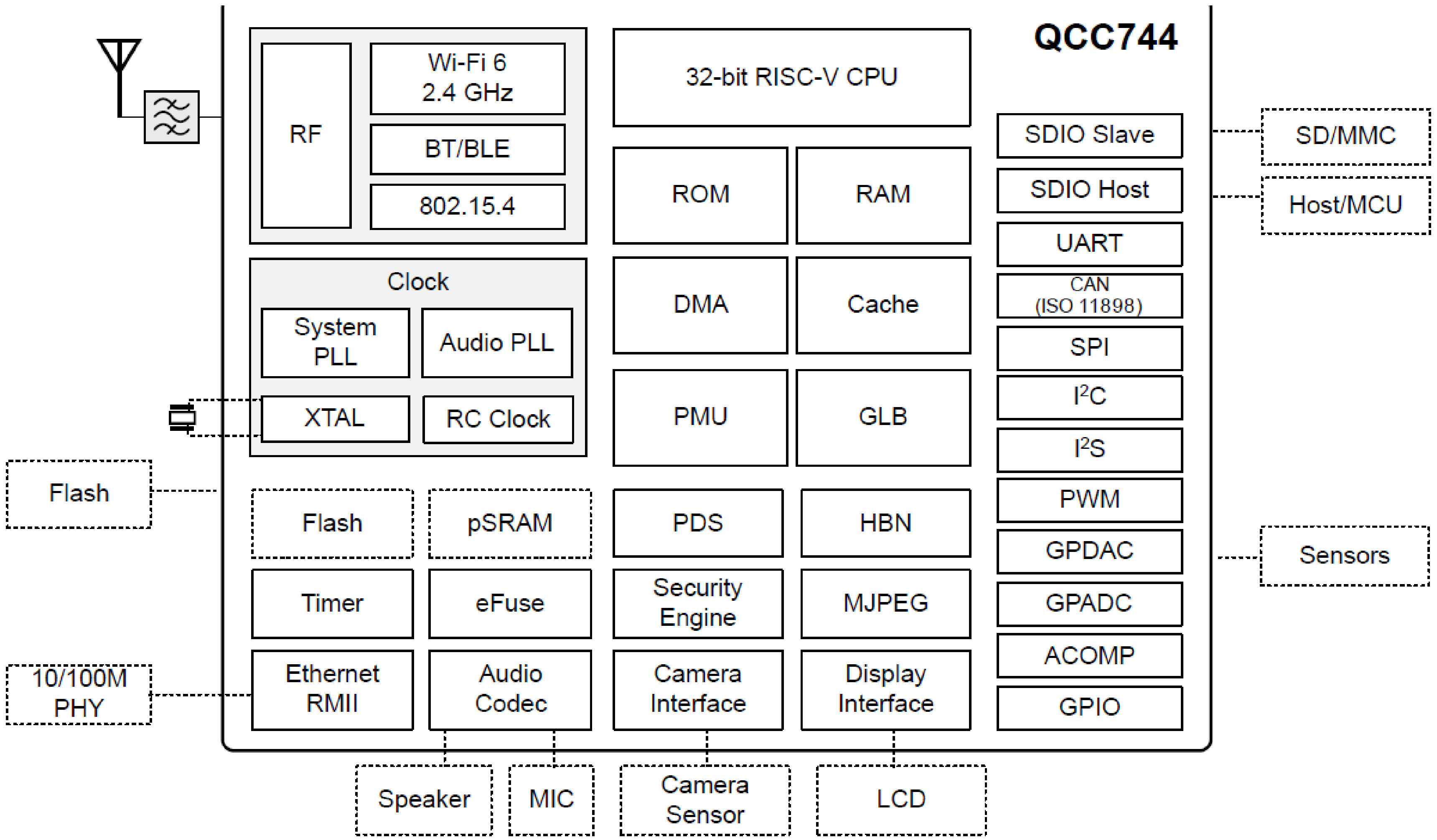
# QCC743 Specification

| Item | Specification | | | |
|---|---|---|---|---|
| **Microcontroller** | - 32-bit RISC-V processor up to 325 MHz | | | |
| **On-chip Memory** | - 484KB SRAM - 128KB ROM - 1/2/4KB OTP - 4Kb eFuse | | | |
| **Security System** | - Security System encryption engine - Secure services (boot, debug, OTA, OTFAD, and so on) | | | |
| **Standard** | - 802.11b/g/n/ax - IEEE 802.15.4 - Bluetooth Classic/Low Energy 5.4 dual mode | | | |
| **Wi-Fi** | • Tx Power (HE40 and MCS9): +15 dBm<br>• Tx Power (HE40 and MCS0): +19 dBm<br>• Tx Power (HE20 and MCS9): +17 dBm<br>• Tx Power (HE20 and MCS0): +19 dBm<br>• Tx Power (DSSS and 1Mbps): +21 dBm<br>• Tx Power (CCK and 11Mbps): +21 dBm | • Rx Sensitivity (HE40 and MCS9): -67 dBm<br>• Rx Sensitivity (HE40 and MCS0): -89 dBm<br>• Rx Sensitivity (HE20 and MCS9): -70 dBm<br>• Rx Sensitivity (HE20 and MCS0): -93 dBm<br>• Rx Sensitivity (DSSS and 1Mbps): -99 dBm<br>• Rx Sensitivity (CCK and 11Mbps): -90 dBm | | |
| **Bluetooth** | **Tx Power**<br>• EDR (3Mbps): +8 dBm<br>• EDR (2Mbps): +8 dBm<br>• BR (1Mbps): +10 dB<br>• BLE (2Mbps): +10 dB<br>• BLE (1Mbps): +10 dB<br>• BLE Coded PHY (500 kbps): +10 dBm<br>• BLE Coded PHY (125 kbps): +10 dBm | **Rx Sensitivity**<br>• EDR (3Mbps): -90 dBm<br>• EDR (2Mbps): -96 dBm<br>• BR (1Mbps): -94 dBm<br>• BLE (2Mbps): -96.5 dBm<br>• BLE (1Mbps): -99 dBm<br>• BLE Coded PHY (500 kbps): -102 dBm<br>• BLE Coded PHY (125 kbps): -105 dBm | | |
| **802.15.4** | • Tx Power (250 Kbps): +19 dBm | • Rx Sensitivity (250 kbps): -105 dBm | | |
| **Peripherals** | 19x configurable I/O: | | | |
| | - Serial Flash<br>- SPI<br>- 11xch 12-bit ADC<br>- 2xch 12-bit-DAC | - SD/MMC<br>- 2x I2C<br>- CAN bus (ISO11898)<br>- I2S | - SDIO 2.0<br>- 2x UART<br>- 4x PWM | - QSPI<br>- JTAG |
| **Voltage** | - Input voltage: 2.97 V~3.63 V<br>- I/O voltage: 1.8 V/3.3 V | | | |

Section 4

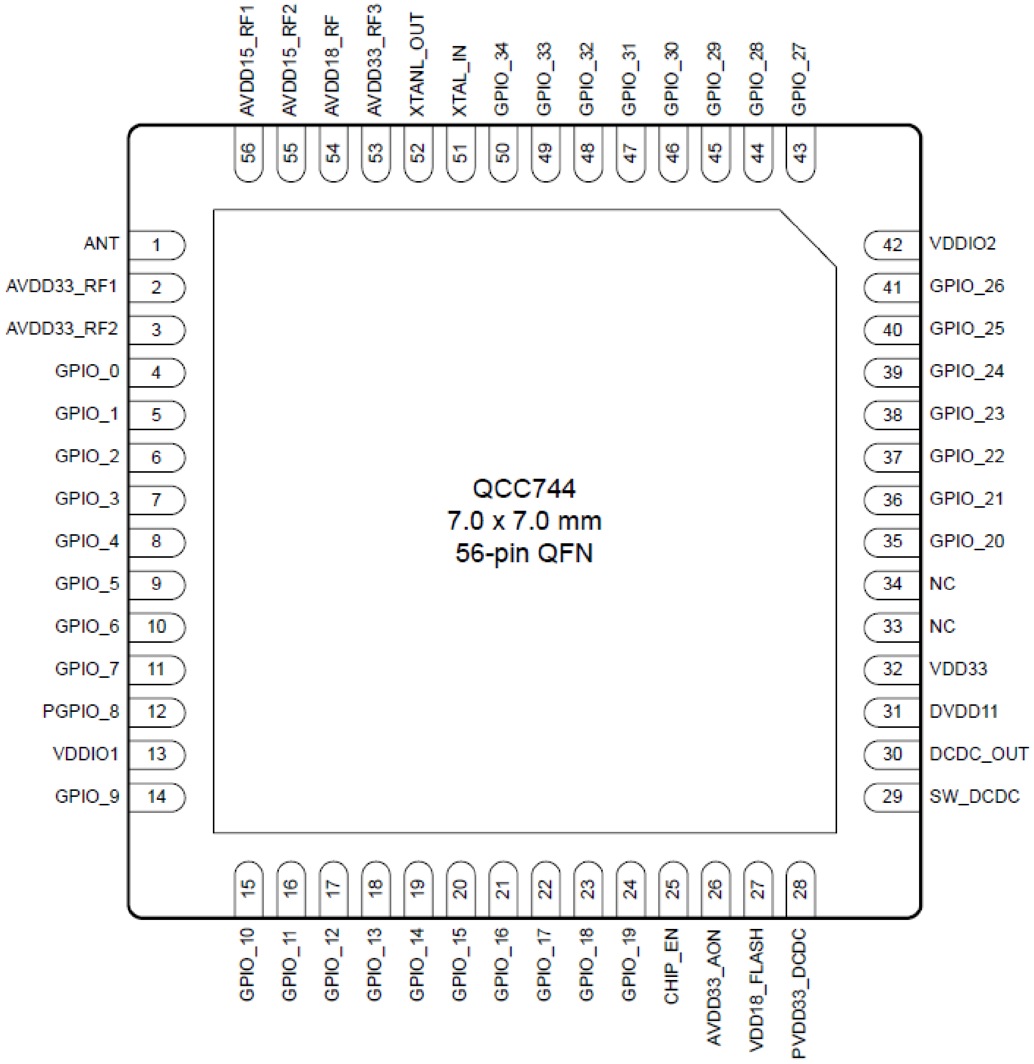
# QCC744 Introduction

# QCC744 Functional Block Diagram



# QCC744 Pin Map

QCC744 56-pin package includes 15 fixed power ports, 4 fixed analog ports, and up to 35 configurable GPIO ports.



# QCC744 Specification

| Item | Specification | | | |
|---|---|---|---|---|
| **Microcontroller** | - 32-bit RISC-V processor up to 325 MHz | | | |
| **On-chip Memory** | - 484KB SRAM - 128KB ROM - 1/2/4KB OTP - 4Kb eFuse | | | |
| **Security System** | - Security System encryption engine - Secure services (boot, debug, OTA, OTFAD, and so on) | | | |
| **Standard** | - 802.11b/g/n/ax - IEEE 802.15.4 - Bluetooth Classic/Low Energy 5.4 dual mode | | | |
| **Wi-Fi** | • Tx Power (HE40 and MCS9): +15 dBm<br>• Tx Power (HE40 and MCS0): +19 dBm<br>• Tx Power (HE20 and MCS9): +17 dBm<br>• Tx Power (HE20 and MCS0): +19 dBm<br>• Tx Power (DSSS and 1Mbps): +21 dBm<br>• Tx Power (CCK and 11Mbps): +21 dBm | • Rx Sensitivity (HE40 and MCS9): -67 dBm<br>• Rx Sensitivity (HE40 and MCS0): -89 dBm<br>• Rx Sensitivity (HE20 and MCS9): -70 dBm<br>• Rx Sensitivity (HE20 and MCS0): -93 dBm<br>• Rx Sensitivity (DSSS and 1Mbps): -99 dBm<br>• Rx Sensitivity (CCK and 11Mbps): -90 dBm | | |
| **Bluetooth** | **Tx Power**<br>• EDR (3Mbps): +8 dBm<br>• EDR (2Mbps): +8 dBm<br>• BR (1Mbps): +10 dB<br>• BLE (2Mbps): +10 dB<br>• BLE (1Mbps): +10 dB<br>• BLE Coded PHY (500 kbps): +10 dBm<br>• BLE Coded PHY (125 kbps): +10 dBm | **Rx Sensitivity**<br>• EDR (3Mbps): -90 dBm<br>• EDR (2Mbps): -96 dBm<br>• BR (1Mbps): -94 dBm<br>• BLE (2Mbps): -96.5 dBm<br>• BLE (1Mbps): -99 dBm<br>• BLE Coded PHY (500 500 kbps): -102 dBm<br>• BLE Coded PHY (125 125 kbps): -105 dBm | | |
| **802.15.4** | • Tx Power (250 Kbps): +19 dBm | • Rx Sensitivity (250 kbps): -105 dBm | | |
| **Peripherals** | 35x configurable I/O: | | | |
| | - 2x Serial Flash<br>- SPI<br>- RMII (10/100M)<br>- 12xch 12-bit ADC | - SD/MMC<br>- 2x I2C<br>- CAN bus (ISO 11898)<br>- 2xch 12-bit DAC | - SDIO 2.0<br>- 2x UART<br>- MIPI-DBI<br>- 4x PWM | - QSPI<br>- I2S<br>- DVP<br>- JTAG |
| **Voltage** | - Input voltage: 2.97 V~3.63 V<br>- I/O voltage: 1.8 V/3.3 V | | | |

# Boot-Strap

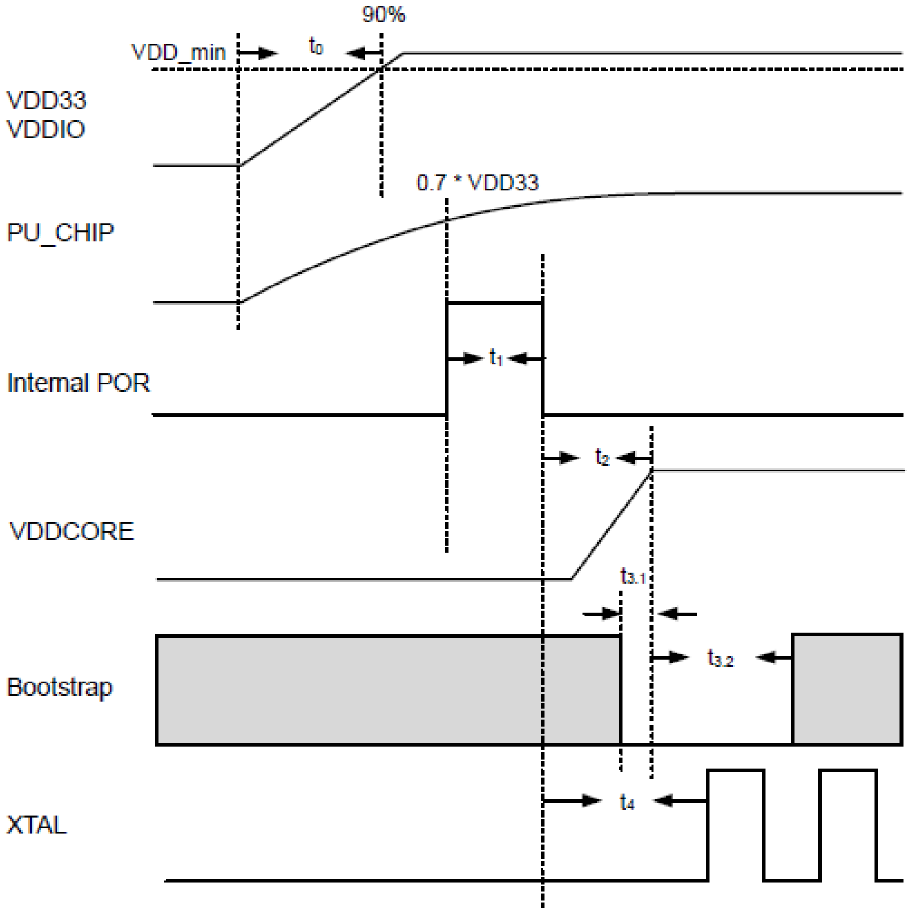
- At each start-up or reset, a chip requires some initial configuration parameters, such as in which boot mode to load the chip, etc.
- These parameters are passed over via the strapping pins.
- GPIO2 and CHIP_EN control the boot mode after the reset is released.

**Boot mode control**

| GPIO2 | CHIP_EN | Boot mode |
|---|---|---|
| 1 | 0->1 | Joint download boot (Boot from UART(GPIO21/22)/SDU) |
| 0 | 0->1 | SPI boot |

# Power up Sequence

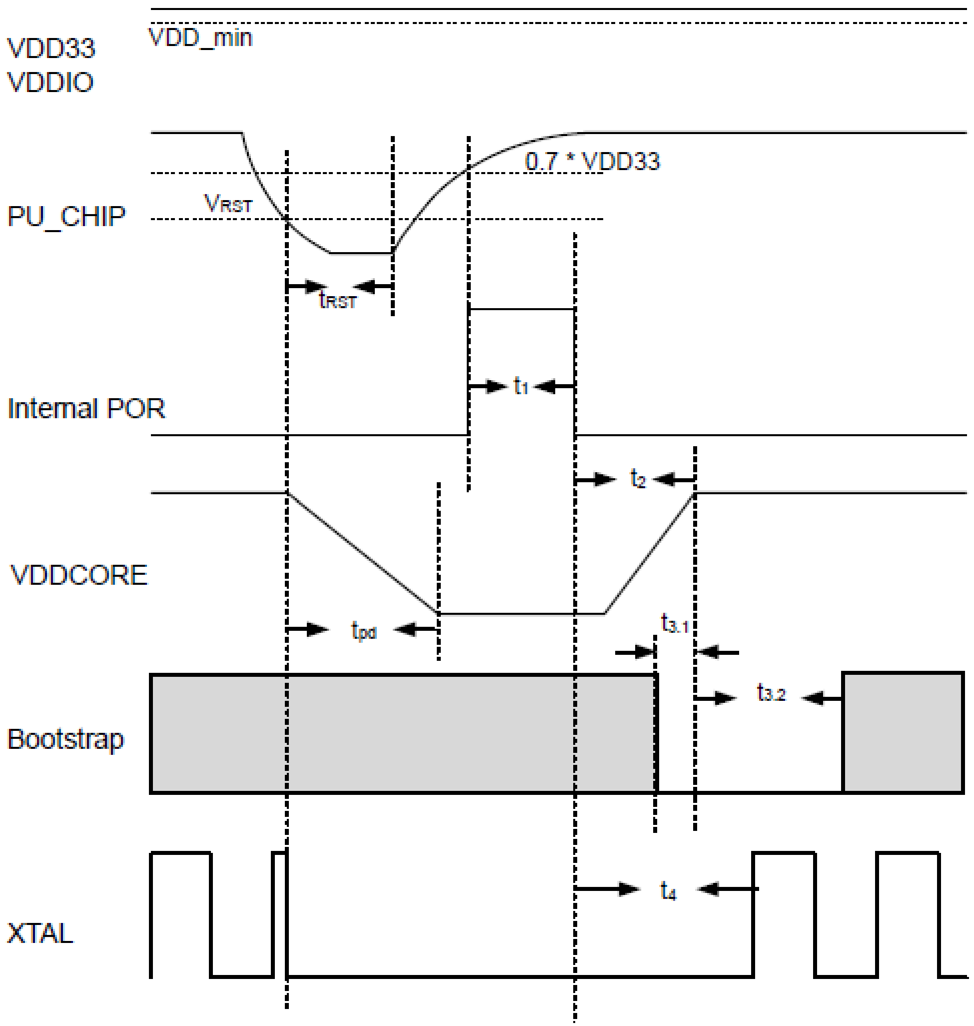
To ensure normal power-on start-up, the power, reset, and bootstrap pins must meet the corresponding timing requirements.




| Parameters | Description | Min.(ms) | Typ(ms) | Max.(ms) |
|---|---|---|---|---|
| $t_0$ | The power supply voltage reaches 90% rise time [a] | - | 0.1 | - |
| $t_1$ | Internal POR duration | - | 3 | - |
| $t_2$ | VDDCORE setting time after Internal POR down | - | 1 | - |
| $t_{3.1}$ | Bootstrap pin [b] preparation time before VDDCORE establishment | 0 | - | - |
| $t_{3.2}$ | Duration of valid voltage level at the bootstrap pin. | 2 | - | - |
| $t_4$ | XTALstartup time after internal POR down | - | 1 | - |

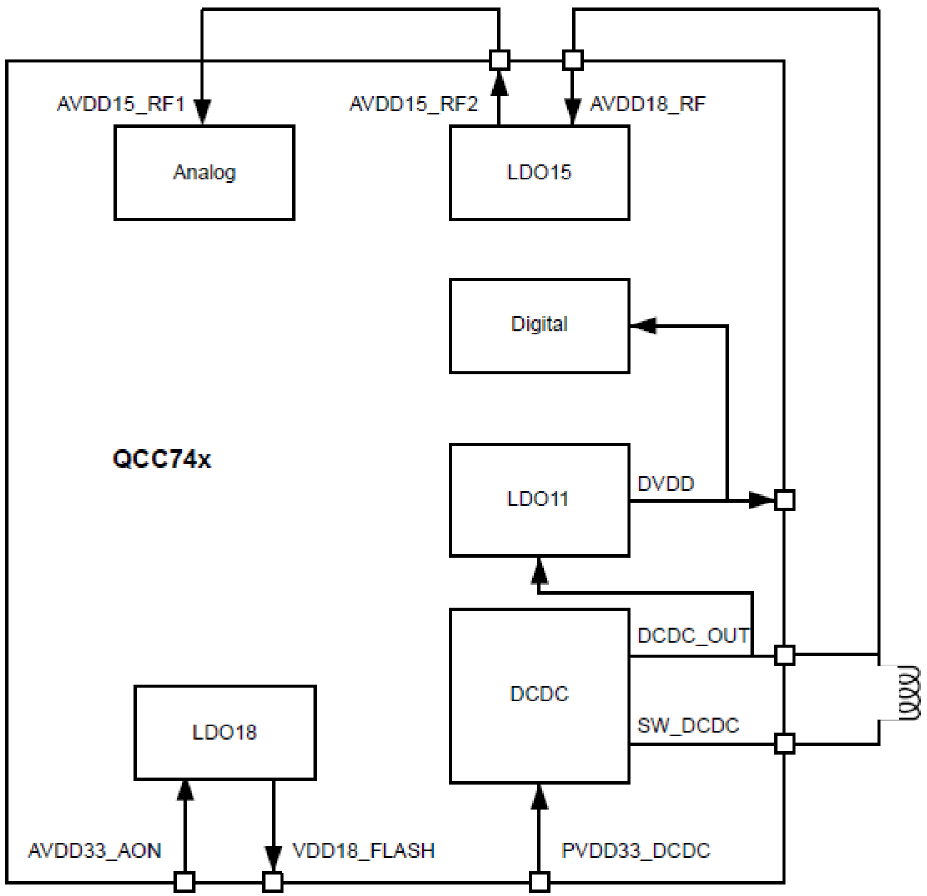
[a] VDD_minis the minimum value for proper chip operation.
[b] Bootstrap pin is GPIO2.

# Shutdown Sequence




| Parameters | Description | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|
| $V_{RST}$ | Shutdown occurs after PU_CHIP lower than this voltage | 0 | 0.1*VDD33 | 0.3*VDD33 | V |
| $t_{RST}$ | The required time that PU_CHIP lower than VRST | 1 | 1 | - | ms |
| $t_{pd}$ | Time for VDDCORE to decrease to 0 after shutdown | 1 | 1 | - | ms |

# Power Block Diagram



Section 5

# QCC74x Hardware Tools

# QCC74x Hardware Tools

## Qconn_Flash

- Qconn_Flash is a UI-based tool used for programming firmware/software image into QCC74x flash memory.
- Path in SDK: qcc74x_sdk/tools/qcc74x_tools/QConn_Flash

## QConn_RCT

- Qconn_RCT is a UI-based tool used for non-signaling/Factory Test Mode performance testing of Wi-Fi/BT/BLE/802.15.4 RF hardware.
- Path in SDK: qcc74x_sdk/tools/qcc74x_tools/QConn_RCT

# QConn_Flash

The **Basic Options** area is used to set communication interface.

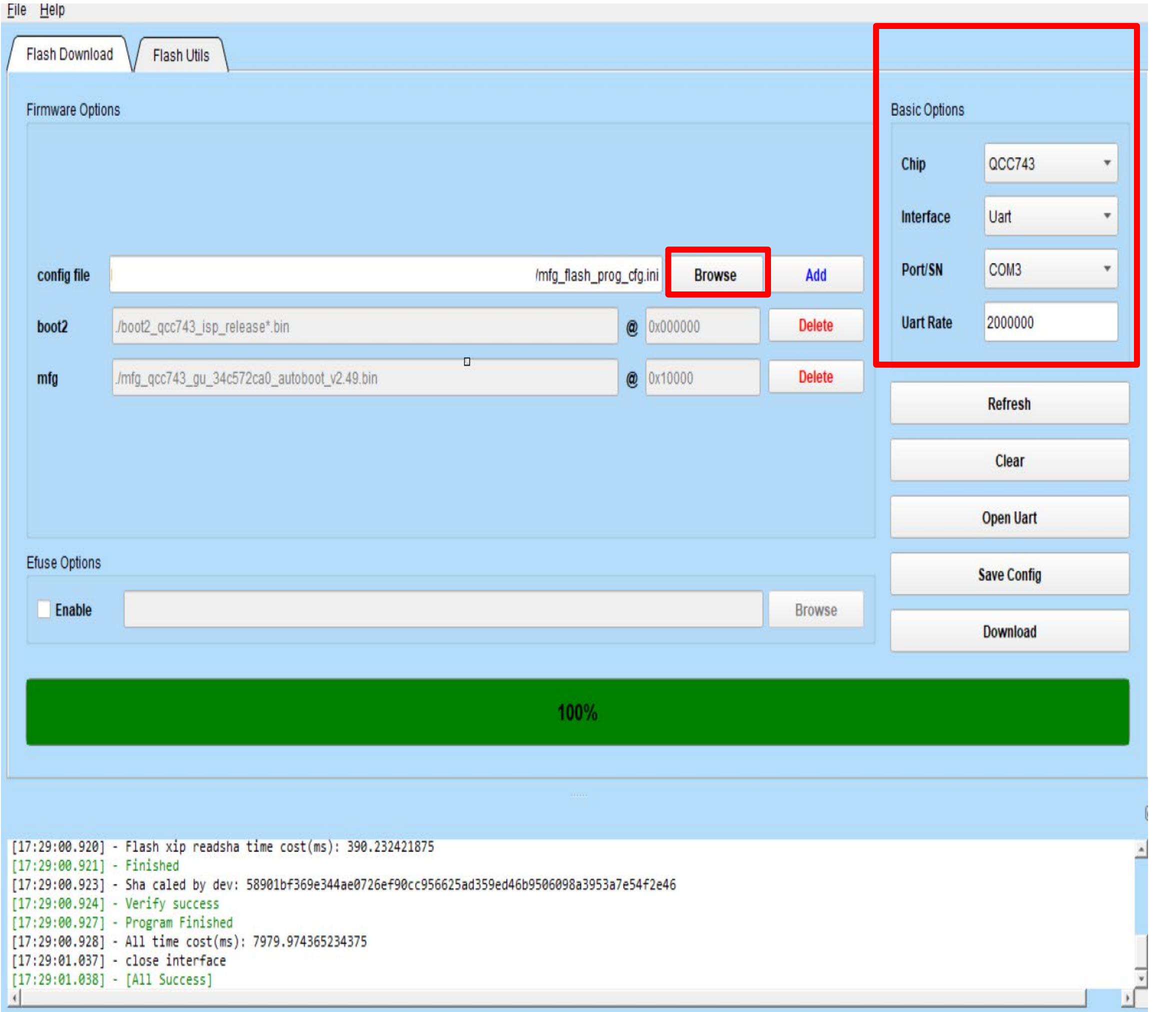
- **Interface**: Select the communication interface Uart for programming
- **Port/SN**: Select the COM number of the module. Click the **Refresh** button to refresh the COM number.
- **Uart Rate**: Set the baud rate of the UART interface. Fill in 2M, which is 2000000.

The **Firmware Options** area is used to select the programming configuration file. After selecting the configuration file for programming through the **Browse** button, the specific programming project and programming address can be displayed.

After completing the preceding interface configuration, enter the module under test into UART start-up mode (UART programming) as follows:

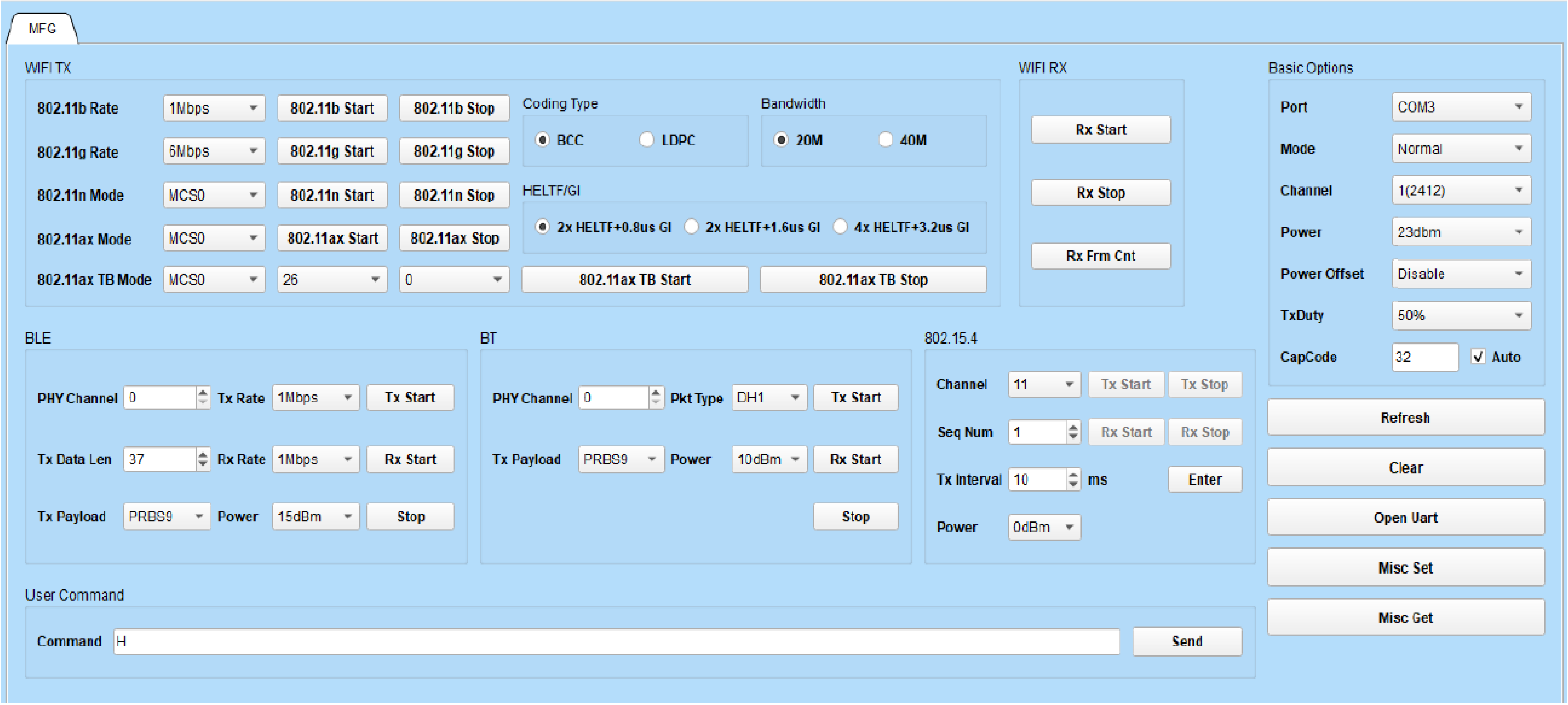
- Press the BOOT_SEL button on the development board, then press the CHIP_EN button
- Release the CHIP_EN button, then release the BOOT_SEL button.

After the module under test switches to UART start-up mode, click the **Download** button in the interface to start programming the MFG test firmware.



# QConn_RCT

QConn_RCT is a UI-based tool for RF performance evaluation test of QCC74x chips and modules.



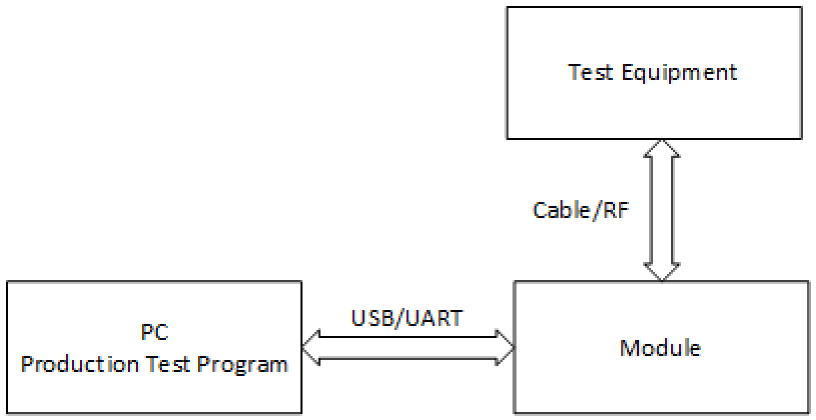
Section 6

# RF Power and XTAL Frequency Offset Calibration

# RF Power and XTAL Frequency Offset Calibration

For RF(WLAN/BT/BLE/802.15.4) power and XTAL frequency offset calibration, CoB or module users must follow the following procedure to obtain the power offset calibration value and frequency offset calibration value and write the power calibration value and frequency calibration value into eFuse memory.

The diagram on the right shows the test environment for production testing/calibration.

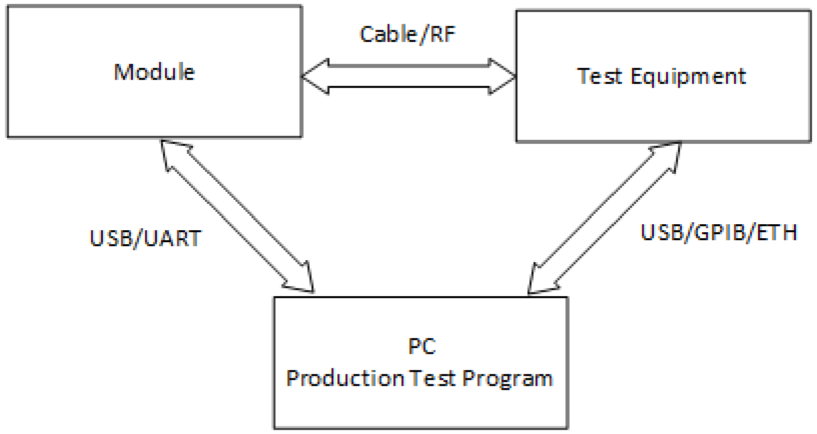



## WLAN RF power offset calibration

- For WLAN RF it is recommended to perform separate calibrations for high power and low power modes across three different channels: high, medium, and low.
- For the remaining channels, a linear interpolation algorithm is used to calculate the calibration values.

## High power mode power calibration

1. Set the power factor to the user-defined target power for the respective mode. For example, if the user sets the target power for 11n mode as Power_Target = 16dBm, set the power factor Power_Code as 16.
2. Measure the actual output power, Pout, and calculate the power deviation for the corresponding channel as Delta_Power = Power_Target - Pout.
3. If the absolute value of Delta_Power is greater than 1, adjust the power factor as Power_Code += Delta_Power (rounding to the nearest integer is required in the actual algorithm). Repeat step 2. If not, proceed to step 4.
4. Calculate the power compensation value for the corresponding channel as Power_Offset_HP[Channel] = (Power_Code - Pout) * 4 (rounding to the nearest integer is required in the actual algorithm).



# RF Power and XTAL Frequency Offset Calibration (cont.)

**Low power mode power calibration**

1. The target power for the low power mode, Power_Target, is fixed at -3dBm (not changeable). Set the power factor, Power_Code, to -3.
2. Measure the actual output power, Pout, and calculate the power deviation for the corresponding channel as Delta_Power = Power_Target - Pout.
3. Calculate the power compensation value for the corresponding channel as Power_Offset_LP[Channel] = (Power_Code - Pout) * 4 (rounding to the nearest integer is required in the actual algorithm).
4. Repeat steps 1 to 3 for the high, medium, and low channels to obtain Power_Offset_LP[3].

**BLE RF power offset calibration**

For BLE power calibration, the 40 channels are divided into 5 groups, where each group shares the same calibration results.

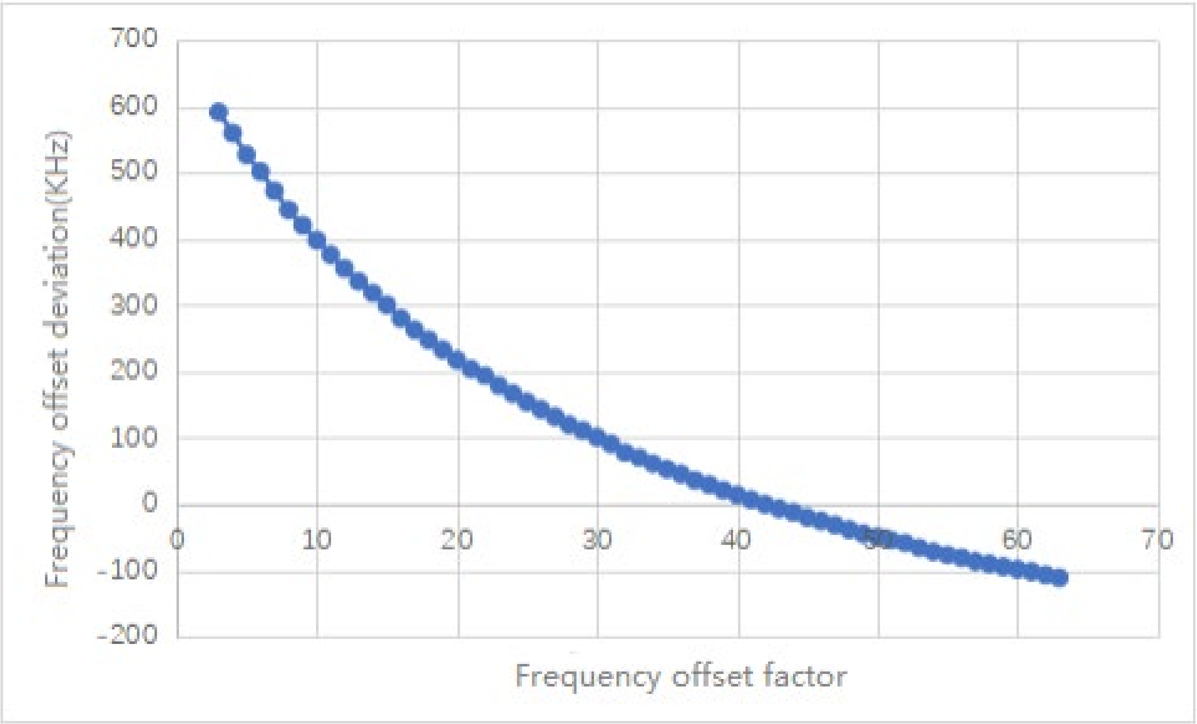
The BT and 802.15.4 modes reuse the calibration results of the nearest BLE channel.

The 40 channels are divided into the following five groups: 2402MHz~2424MHz, 2426MHz~2440MHz, 2442MHz~2456MHz, 2458 MHz~2472 MHz, 2474MHz~2480MHz.

1. Set the power factor to the user-defined target power for the respective mode. For example, if the user sets the target power for 1Mbps mode as Power_Target = 10 dBm, set the power factor Power_Code as 10.
2. Measure the actual output power, Pout, and calculate the power deviation for the corresponding channel as Delta_Power = Power_Target - Pout.
3. Calculate the power compensation value for the corresponding channel as Power_Offset_BLE[Channel] = (Power_Code - Pout) * 4 (rounding to the nearest integer is required in the actual algorithm).
4. Repeat steps 1 to 3 for all channels 5, 15, 23, 31, and 37 to obtain the power factor compensation array for the corresponding group of channels, Power_Offset_BLE[5].

# RF Power and XTAL Frequency Offset Calibration (cont.)

The QCC74x series chips have an integrated capacitor bank for frequency offset compensation, capacitor bank is programmed to adjust the frequency deviation of the external crystal. The frequency offset factor ranges from 0 to 63, and there is a roughly linear and monotonically decreasing relationship between the frequency offset factor and the frequency offset value. Please refer to the diagram for a specific example.




1. Set the frequency offset factor Capcode to 0x20.
2. Set the algorithm loop index to 4.
3. Read the frequency offset value Freq_Offset from the instrument.
4. If the frequency offset value Freq_Offset is within the calibration range, calibration is complete. Record the current frequency offset factor. Otherwise, proceed to step 5.
5. If the frequency offset value Freq_Offset is positive, modify the frequency offset factor Capcode by adding 2^ index. Otherwise, modify the frequency offset factor Capcode by subtracting 2^index. Also, decrement the algorithm loop index by 1.
6. Repeat steps 3 to 5 until the algorithm loop index becomes 0.

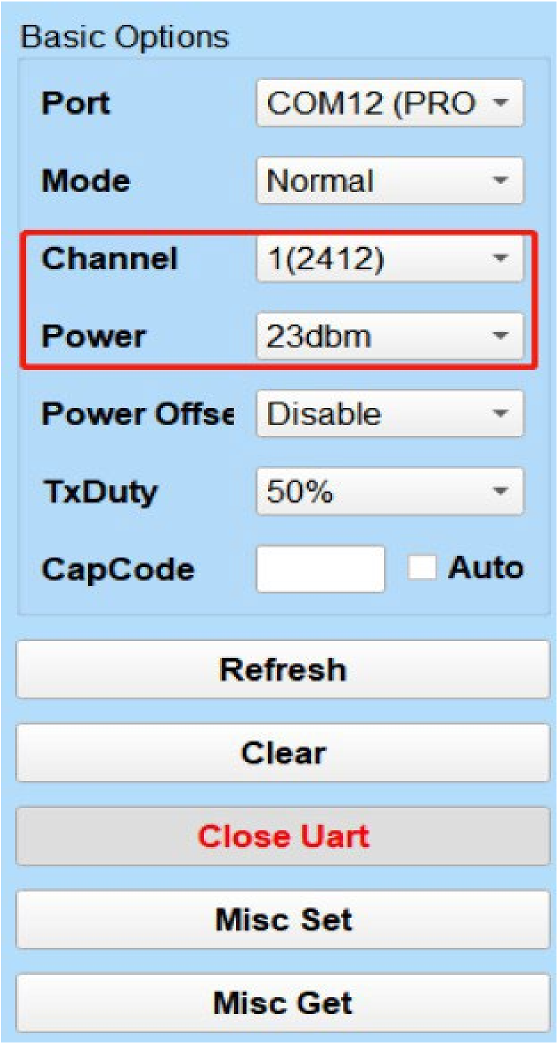
Section 7

# RF Testing and Calibration

# Channel and Power settings

**Channel and Power settings**

1. Through the Channel and Power drop-down option boxes, you can set the transmission channel and transmission power of Wi-Fi data packets.
2. The Channel selection range is 1-14,
3. The Power selection range is -15 dBm ~ 23 dBm.
4. If the module to be tested has been calibrated for production testing, you can select Enable for Power Offset and Auto for CapCode, then click Misc Get first, and then click Misc Set to set the production calibration data to the chip's internal registers.



# Wi-Fi Testing

**Setting for transmitting Wi-Fi 802.11b packets**

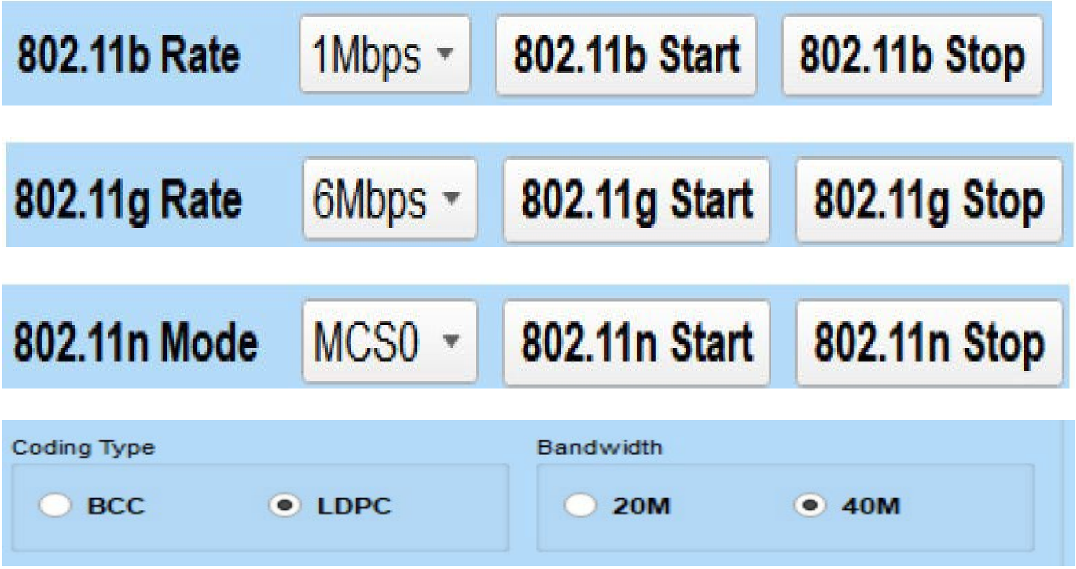
1. The 11b data packet can choose from the rate: 1Mbps, 2Mbps, 5.5Mbps, 11Mbps, and long preamble is used by default.
2. After setting up 11b data packet, click the 802.11b Start button to start transmitting 11b data packets.
3. To stop transmitting 11b data packet, click the 802.11b Stop button.

**Setting for transmitting Wi-Fi 802.11g data packets**

1. The rate of 11g data packets can be selected are: 6Mbps, 9Mbps, 12Mbps, 18Mbps, 24Mbps, 36Mbps, 48Mbps, 54Mbps.
2. After setting up 11g data packet, click the 802.11g Start button to start transmitting 11g data packets.
3. To stop transmitting, click the 802.11g Stop button.

**Settings for transmitting Wi-Fi 802.11n packets**

1. For transmitting 11n data packets, the rate can be chosen from MCS0-MCS7 data rates.
2. Bandwidth can be selected is either 20 MHz or 40 MHz.
3. The encoding method can be chosen is either BCC or LDPC.
4. The data packets sent by 11n are all in Long GI, HT- MF format.
5. Note: Currently HT_GF mode is not supported.
6. After settings are completed.
7. Please click the 802.11n Start button to start transmitting 11n data packets.
8. To stop transmitting, click the 802.11n Stop button.



# Wi-Fi Testing (cont.)

**Settings for transmitting Wi-Fi 802.11ax packets**

1. For transmitting 11ax data packet can choose the rate options as MCS0-MCS9, DCM-MCS0, DCM-MCS1, DCM- MCS3, DCM-MCS4, ER-MCS0~ER-MCS2
2. Bandwidth can be selected is either 20 MHz or 40 MHz.
3. The encoding method can be chosen is either BCC or LDPC.
4. The HE-LTF/GI options are 2x HELTF+0.8us, 2x HELTF+1.6us, 4x HELTF+3.2us
5. After settings are completed.
6. Please click the 802.11ax Start button to start transmitting 11n data packets.
7. To stop transmitting, click the 802.11ax Stop button



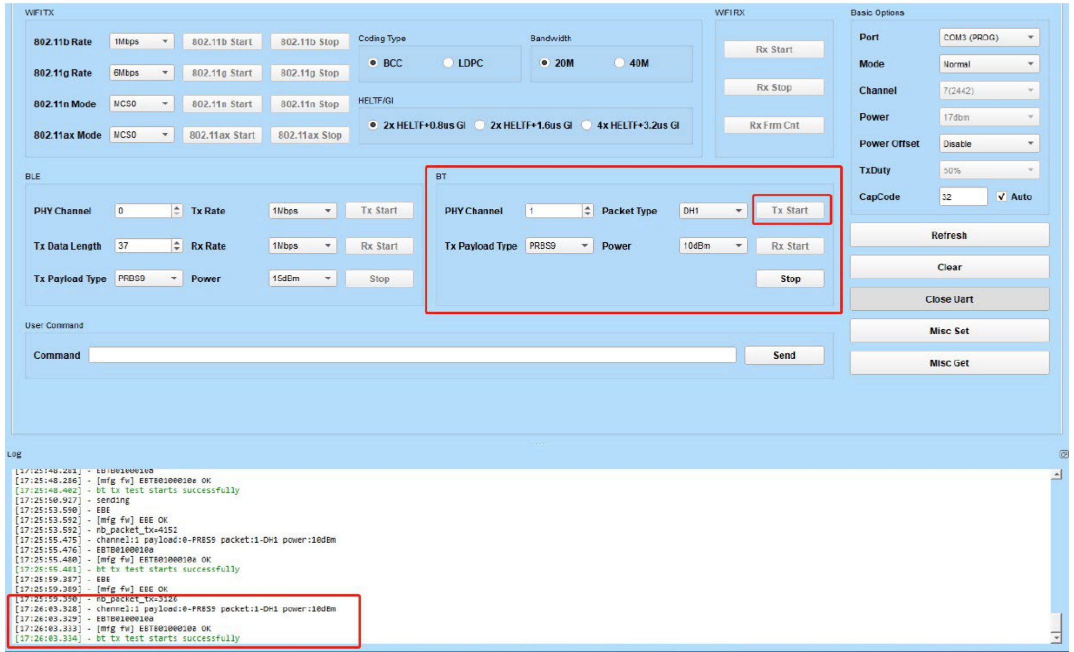
**Setting for receiving Wi-Fi packets**

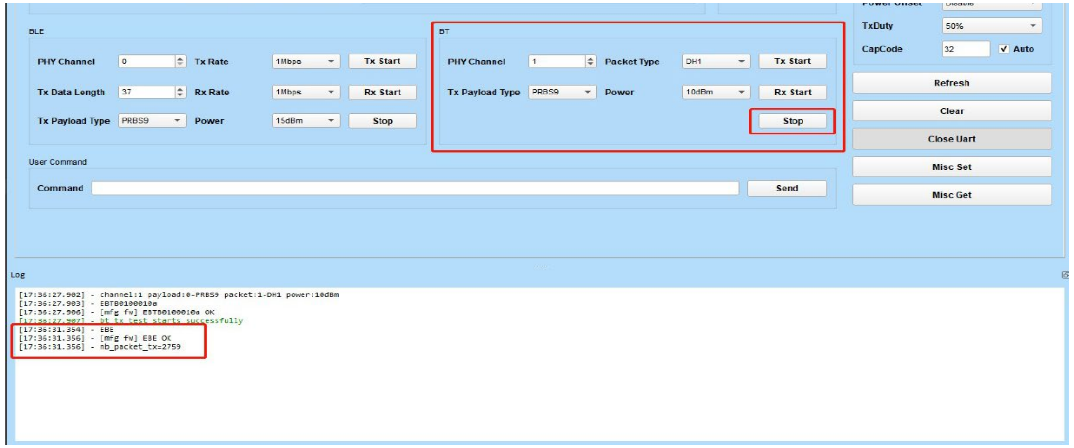
1. Click the Rx Start button to enter Wi-Fi data packet reception mode.
2. Click the Rx Frm Cnt button to display the number of data packets received so far and the average RSSI of the data packets.
3. NOTE: Before starting to test the reception performance, manually stop the transmission performance test

# BT Testing

**Settings for transmitting BT packets**

1. For transmitting BT packet, please select the required PHY Channel, Packet Type, Tx Payload Type and Power.
2. click the Tx Start to enter BT transmit mode.
3. When bt tx test starts successfully appears in the Log window, it means that BT enters the transmitting mode successfully, as shown in the figure.
4. To stop transmitting BT packets, click the Stop button.
5. When nb_packet_tx = xxxx appears in the Log window, it means that the stop is successful and the number of data packets sent is displayed, as shown in the figure.

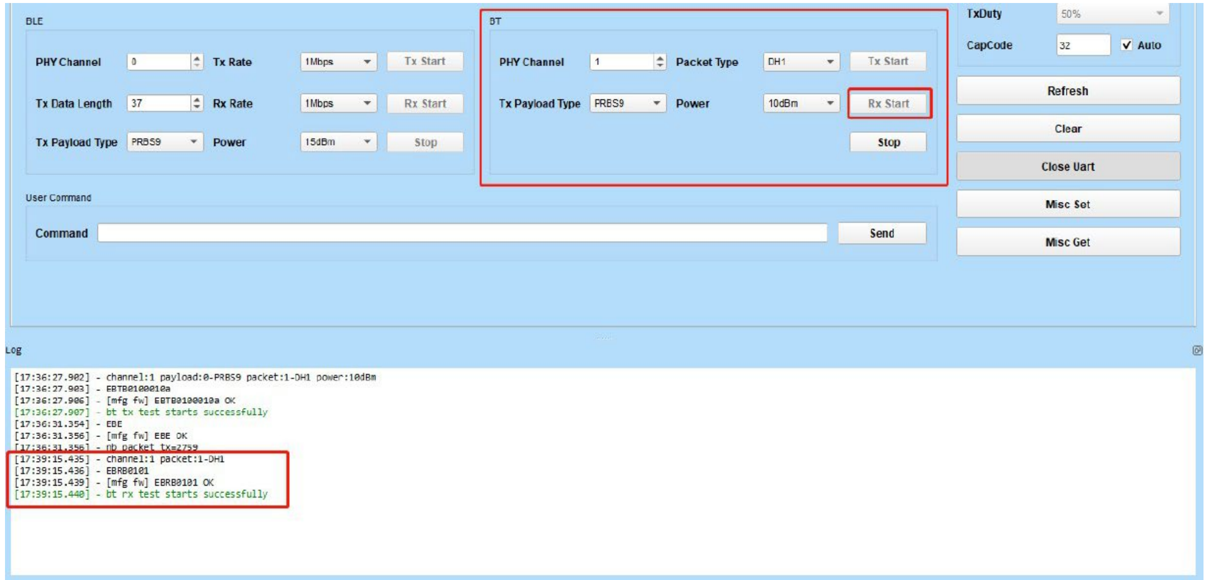


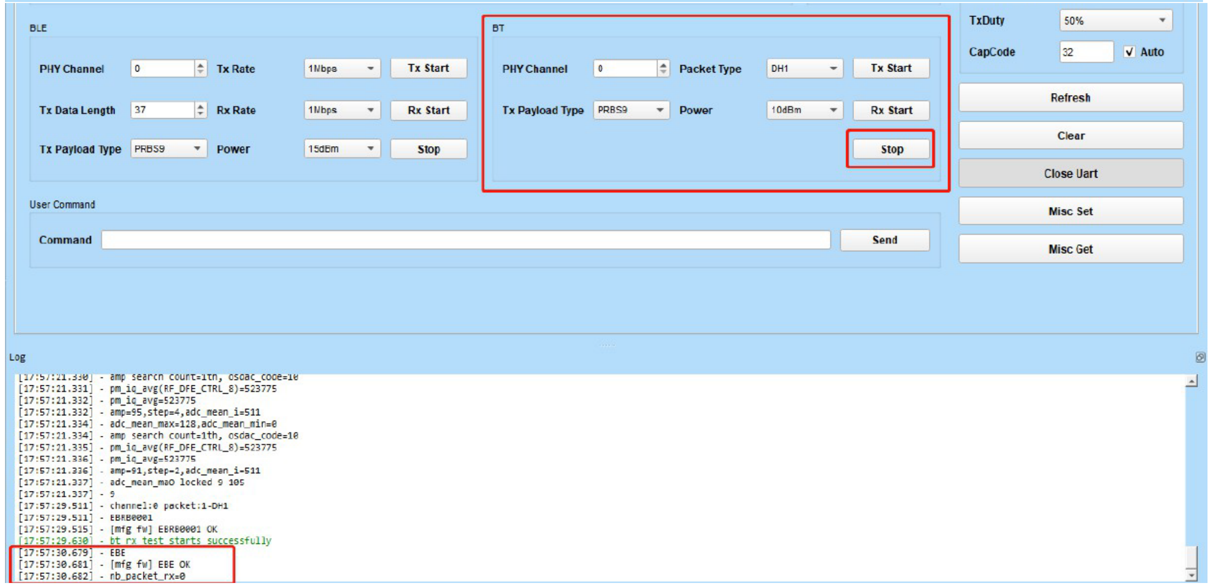



# BT Testing (cont.)

**Settings for receiving BT packets**

1. BT can only receive DH packets with BD_ADDR 0.
2. When BT receives, select the required PHY Channel, Packet Type,
3. click the Rx Start to enter the data packet receiving mode.
4. When bt rx test starts successfully appears in the Log window, it means that BT enters the receiving mode successfully, as shown in the figure.
5. To stop BT receive, use the Stop button.
6. When nb_packet_rx=xxxx appears in the Log window, it means that the stop is successful and the number of received data packets is displayed, as shown in the figure.

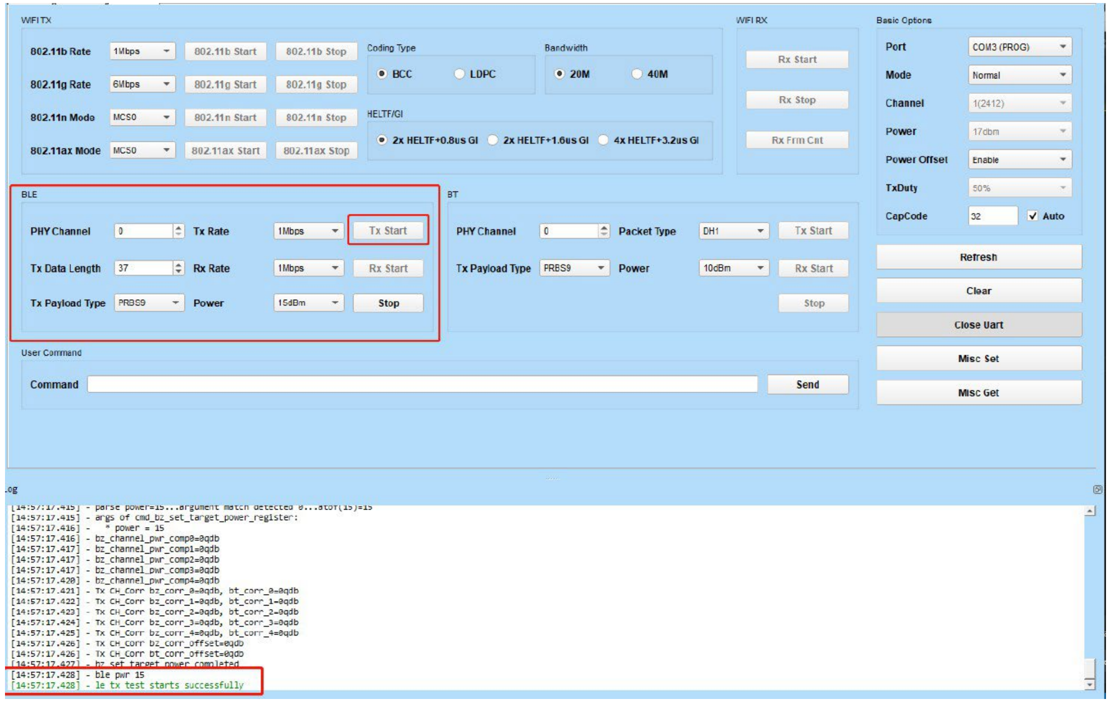


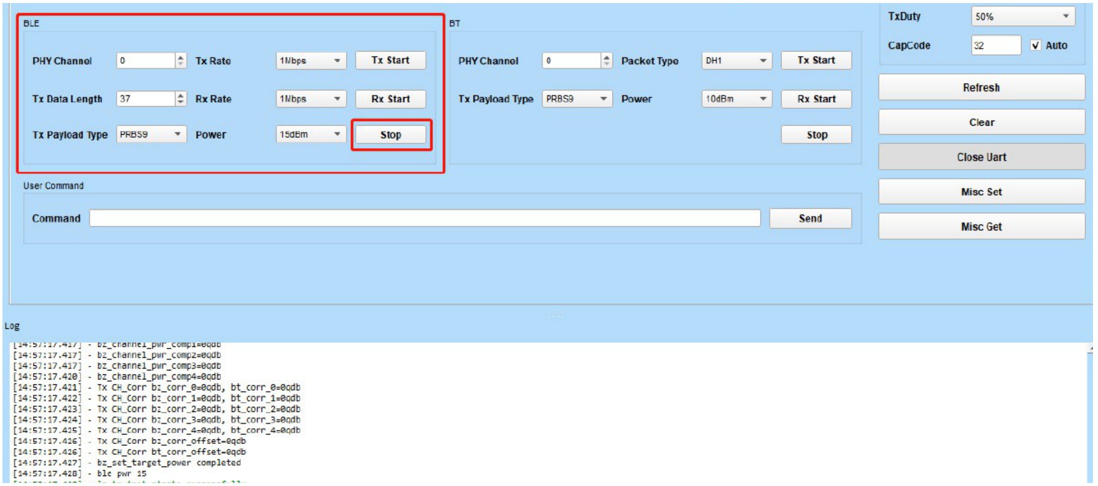



# BLE Testing

**Settings for transmitting BLE packets**

1. For transmitting BLE data packet, please select the required PHY Channel, Tx Rate, Tx Data Length, Tx Payload Type, and Power.
2. Click the Tx Start button to enter the BLE data packet transmission mode.
3. When the “Ble tx test starts successfully” message appears in the Log window, it means that the BLE has successfully entered the transmission mode, as shown in the figure.
4. To stop transmitting BLE data packets, click the Stop button.
5. When le test stopped appears in the Log window, it means that the transmission is stopped successfully, as shown in the figures.

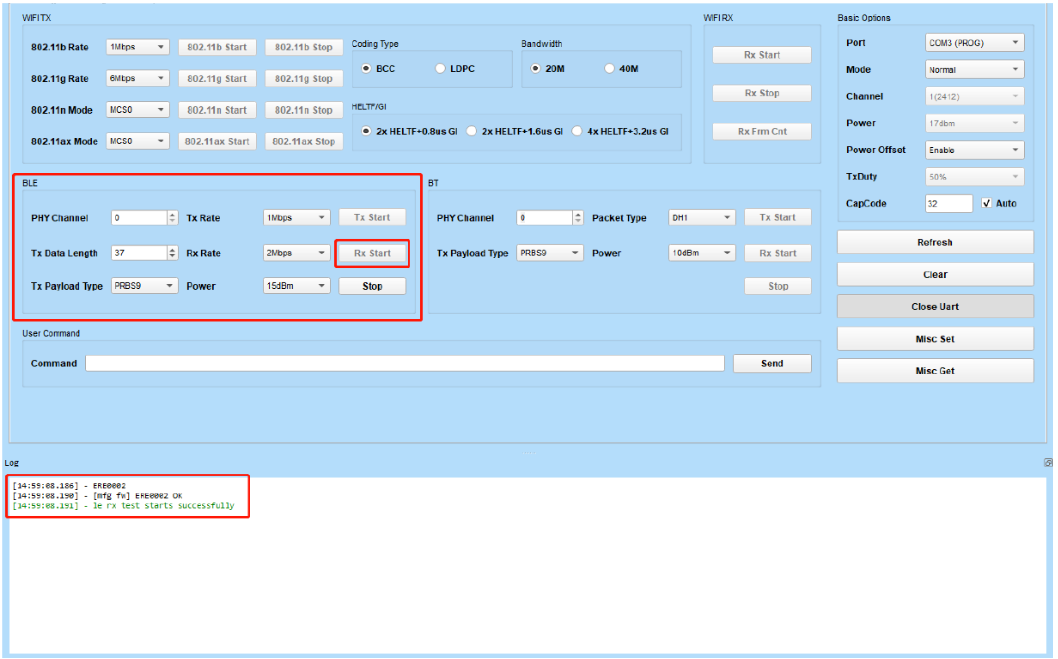


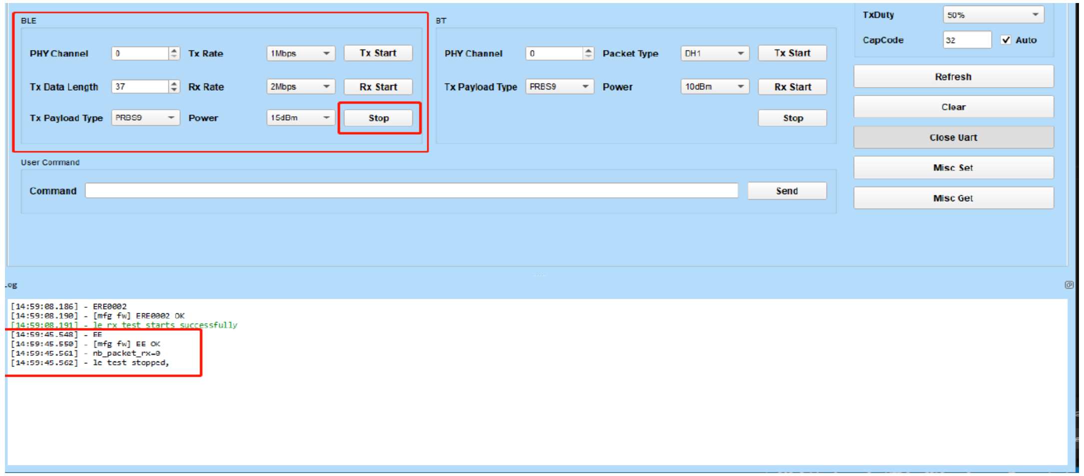



# BLE Testing (cont.)

**Settings for receiving BLE packets**

1. To receive a BLE data packet, select the required PHY Channel, Rx Rate to be tested.
2. Then click the Rx Start button to enter the receiving mode of BLE data packets. When the message “Ble rx test starts successfully” appears in the Log window, it means that BLE successfully enters the receiving mode, as shown in the figure.
3. To stop receiving BLE data packet, click the Stop button, and the number of received data packets will be displayed in the Log window, as shown in the figure.

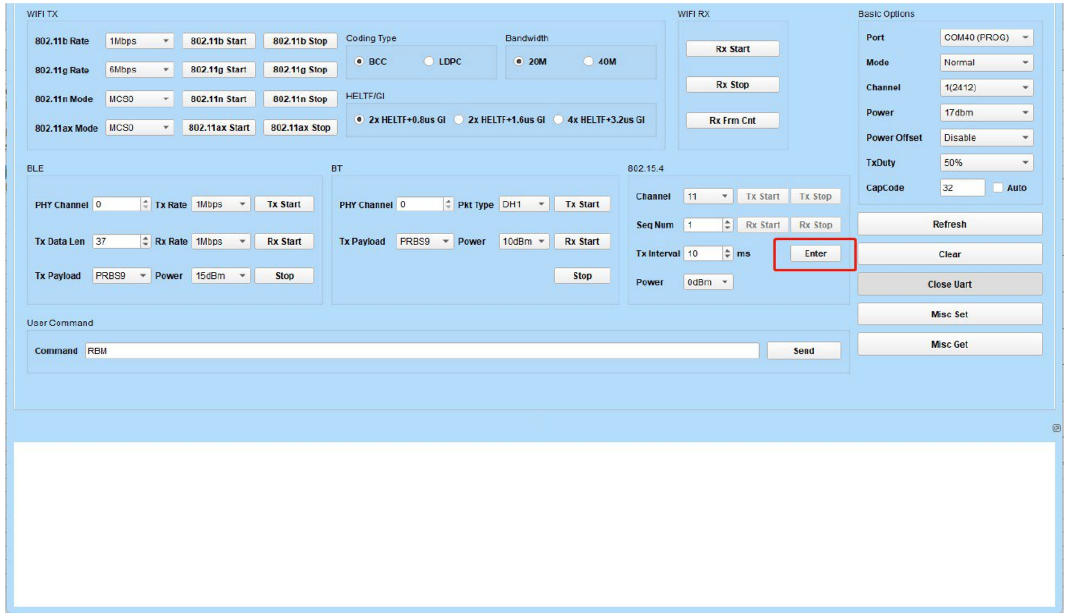


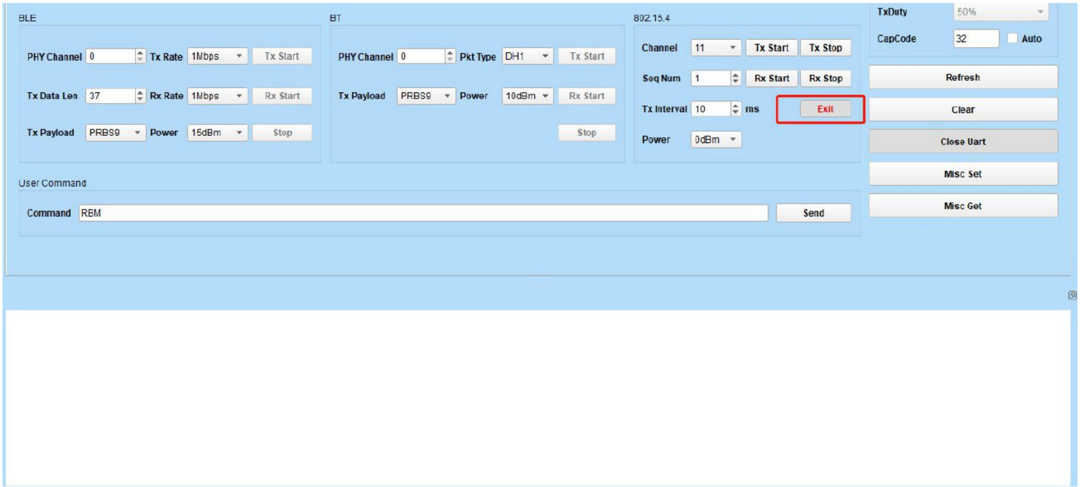



# 802.15.4 Testing

**Settings to configure QCC74x in 802.15.4 non-signaling mode**

1. Click the Enter button to enter the 802.15.4 non-signaling test mode, as shown in the figure.
2. Click the Exit button to exit from the 802.15.4 non-signaling test mode, as shown in the figures.



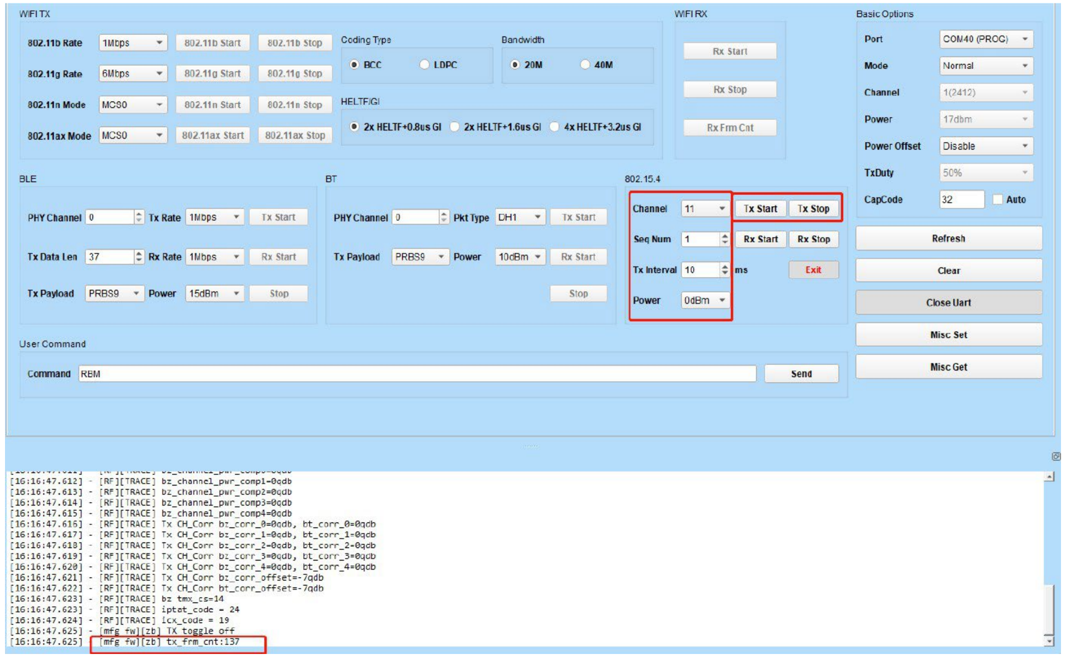
# 802.15.4 Testing (cont.)

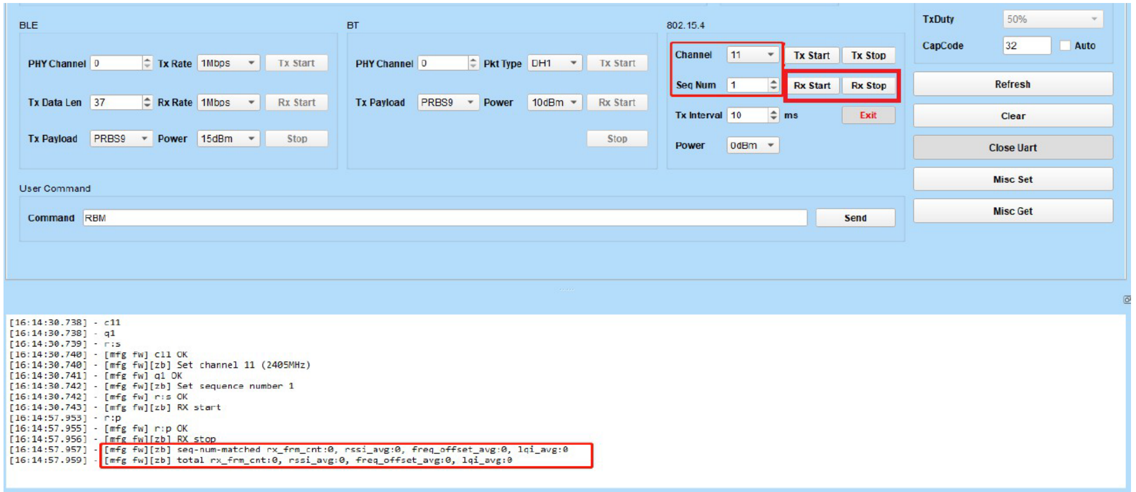
**Settings for transmitting 802.15.4 packets**

1. After entering the 802.15.4 non-signaling test mode, set the required Channel, Seq Num and Tx Interval, Power.
2. Click the Tx Start button to start transmitting the packets.
3. Click Tx Stop to stop transmitting the packets. After the test is completed, the number of sent packets will be displayed in the Log window.

**Settings for receiving 802.15.4 packets**

1. After entering the 802.15.4 non-signaling test mode, set the required Channel and Seq Num.
2. Click the Rx Start button to start the test.
3. Click the Rx Stop button to end the test. After the test is completed, the number of successfully received packets, as well as the average RSSI Frequency Offset and LQI will be displayed in the Log window.



Section 8

# Documentation

# Hardware Documents

| DCN | Title | Status |
|---|---|---|
| 80-WL743-1 | QCC743/QCC744 Data Sheet | Released |
| 80-WL740-3 | QCC74x Layout Design Guidelines | Released |
| 80-WL740-5 | QCC74x Hardware Training Guide | Released |
| 80-WL740-8 | QCC74x Hardware Design Guidelines | Released |
| 80-WL740-20 | QCC74x Evaluation Kit User Guide | Released |
| 80-WL740-41 | QCC74x Reference Schematic | Released |
| 80-WL740-71 | QCC74x Design Verification Test Report | Released |
| 80-WL740-12 | QCC743 Thermal Analysis Standard JEDEC Thermal Simulation Report | Released |
| 80-WL740-13 | QCC744 Thermal Analysis Standard JEDEC Thermal Simulation Report | Released |
| 80-WL740-7 | QCC74x Manufacturing User Guide | Released |
| DP25-WL740-1 | Design Package, QCC743 QCC744 Hostless Sample Design | Released |

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