Qualcomm Technologies, Inc.

QCC743 Thermal Analysis

Standard JEDEC Thermal Simulation Report

80-WL740-12 Rev. AB

March 3, 2025

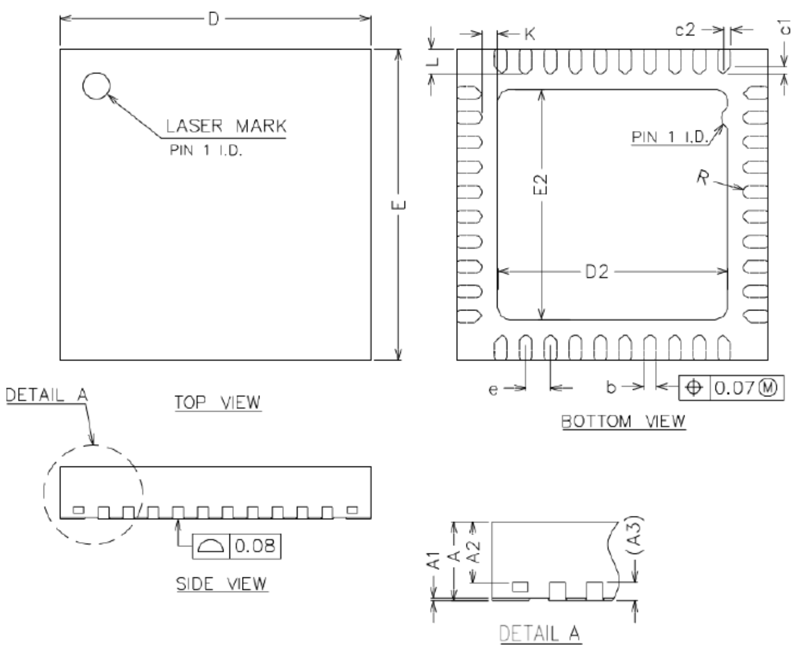
1 Introduction

This thermal simulation report is aimed to evaluate the thermal performance of QCC743. The software Icepak is utilized.

2 Simulation conditions

PCB type	Symbol	Definition	Unit
4 layers (2s2p)	$R_{\Theta JA}$	Thermal resistance, junction to ambient environment (natural convection)	°C/W
4 layers (2s2p)	$R_{\Theta JB}$	Thermal resistance, junction to board (forced convection)	°C/W
-	$R_{\Theta JC}$	Thermal resistance, junction to case (forced convection)	°C/W
4 layers (2s2p)	Ψ_{JT}	Thermal property parameter, junction to top thermal (forced convection)	°C/W

3 Package model



UNITS OF MEASURE=MILLIMETER

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.075	–	–
c1	–	0.12	–
c2	–	0.12	–

Figure 1 QCC743 QFN-40 package drawing

4 Material properties and structure parameters

Table 1 Thermal properties of component material

Component	Material	Size (mm×mm×mm)	Thermal conductivity (W/m.K)
EMC	EMEG700QB	5×5×0.85	0.96
Die	Silicon	3.2993×3.2993×0.15/ 1.13×1.24×0.15	148
DAF	HR-5104T-25	1.13×1.24×0.025	0.3
DAA	EN4900GC	3.2993×3.2993×0.02	2
Leadframe	Copper	Import	386

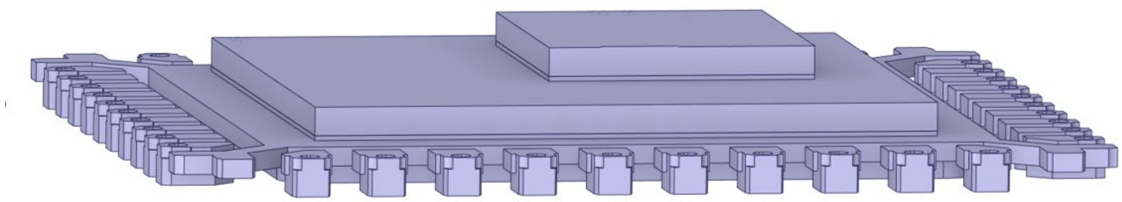


Figure 2 3D structure

Table 2 Thermal resistance data

Power	PCB type	Convection type	Ambient temperature	T_J (J_A) ℃	Θ_{JA} ℃/W	T_J (J_B) ℃	Θ_{JB} ℃/W	T_J (J_C) ℃	Θ_{JC} ℃/W
1W/ 0.054W	2S2P	Natural convection	25℃	68.7245	41.48	62.5726	35.64	51.4988	25.14

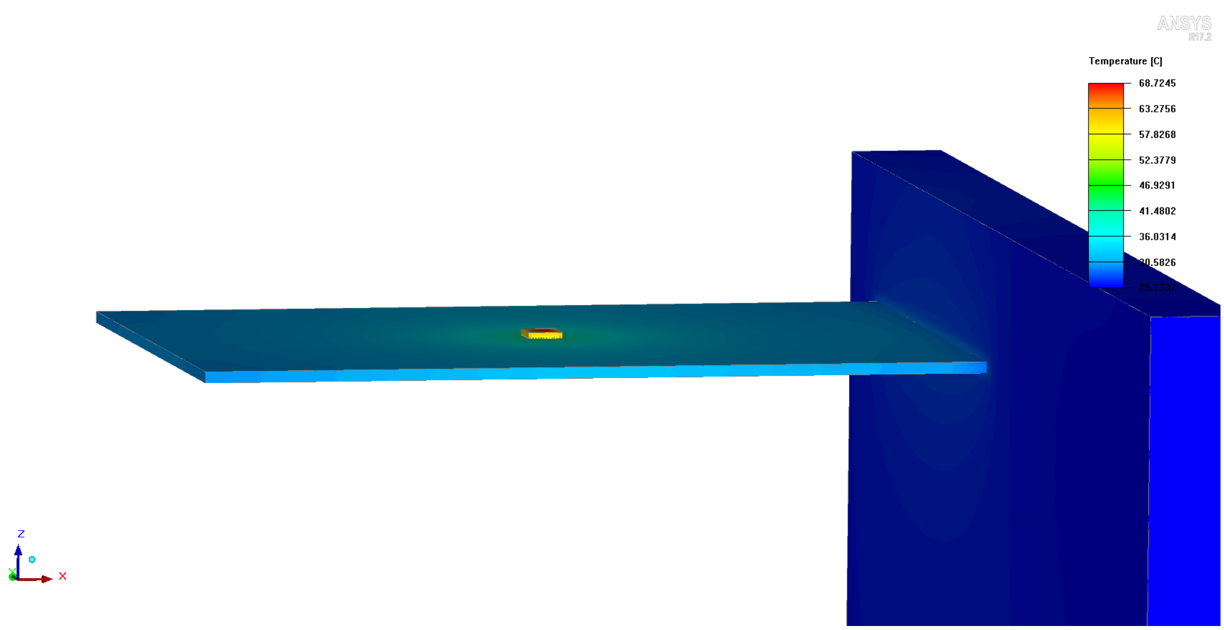


Figure 3 Thermal resistance of θ_{JA}

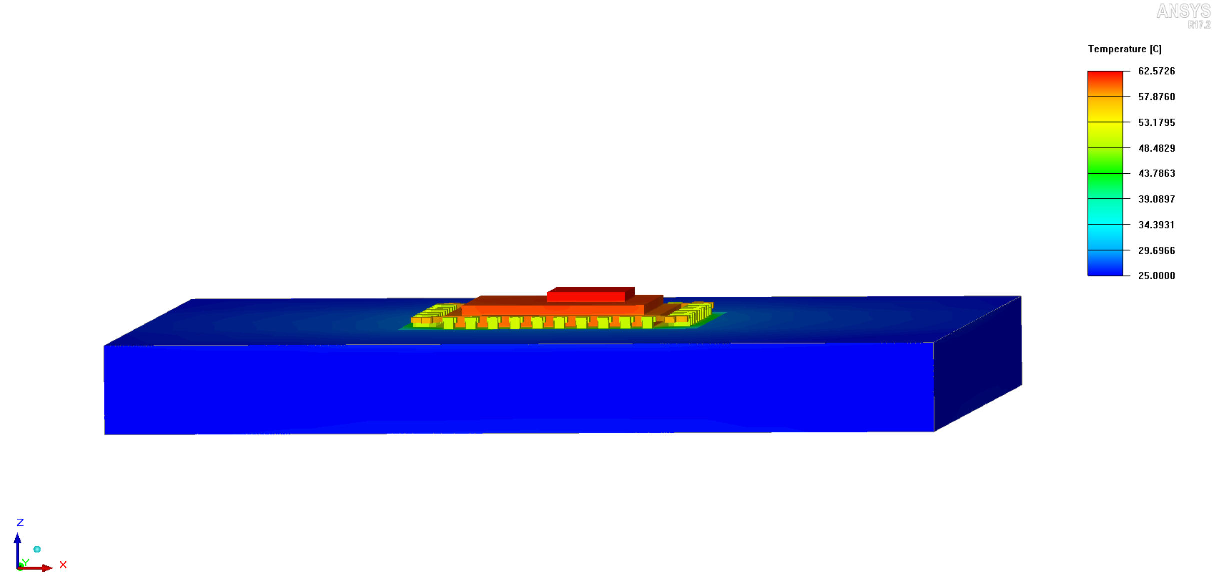


Figure 4 Thermal resistance of θ_{JB}

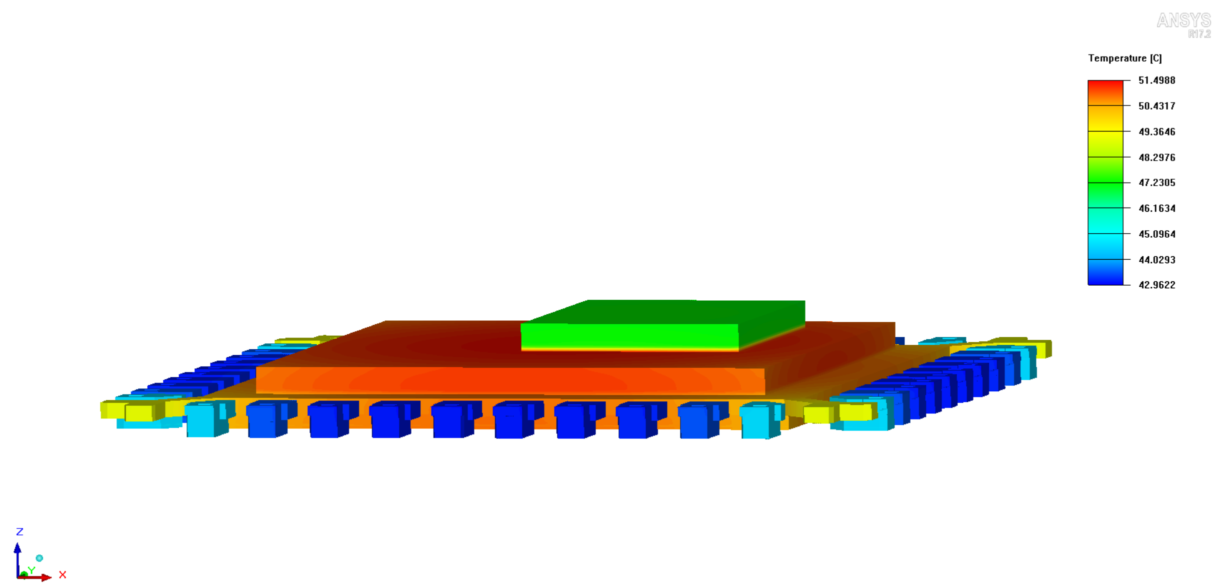


Figure 5 Thermal resistance of θ_{JC}

A Appendix

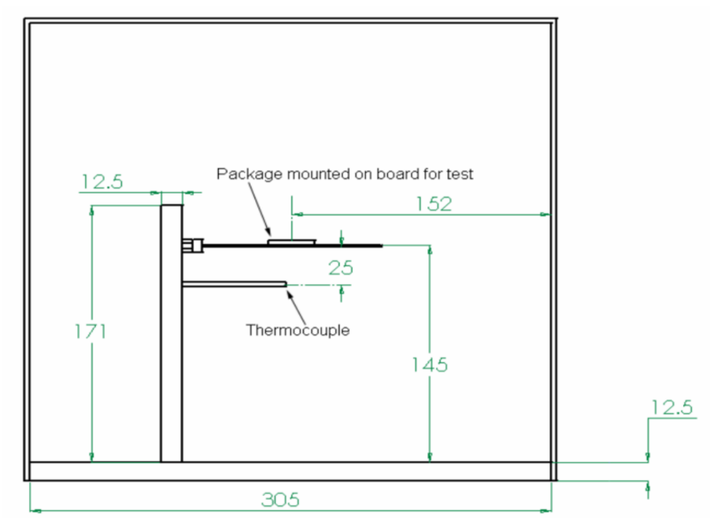
- θ_{JA} Junction to ambient thermal resistance:

  $\theta_{JA} = (T_{J,MAX} - T_A) / P_H$

  Where $T_{J,MAX}$ = maximum junction temperature.

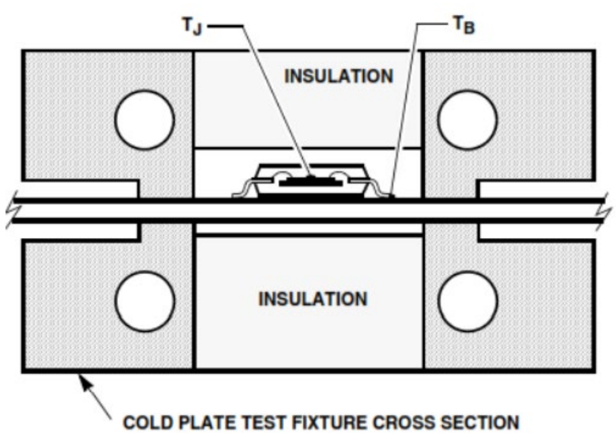
  T_A = ambient temperature
  P_H = total power dissipation

  θ_{JA} represents the resistance of the heat flows from the chip to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance.



- θ_{JB} Junction to board thermal resistance:

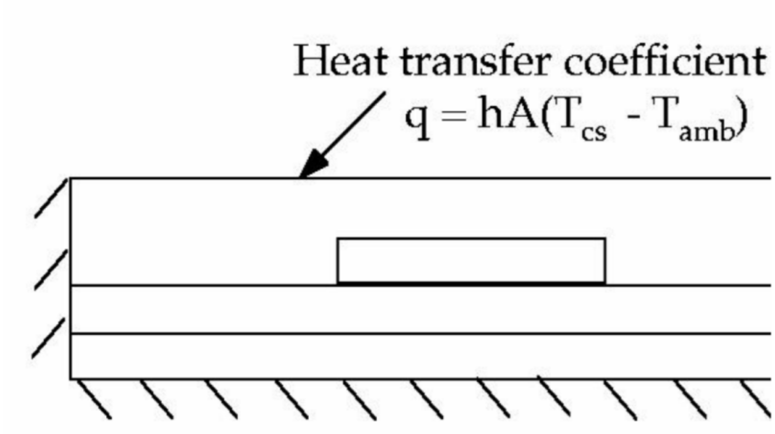
  $\theta_{JB} = (T_{J,MAX} - T_{BOARD}) / P_H$
  Where T_{Board} is the temperature measured on or near the component lead or solder, using a 2s2p board



- θ_{JC} Junction to case thermal resistance:

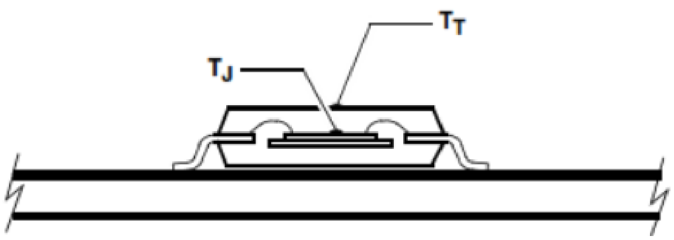
  $\theta_{JC} = (T_{J,MAX} - T_C) / P_H$

Where T_C = case temperature which is monitoring on package surface
θ_{JC} represents the thermal resistance between the chip to package top case. θ_{JC} is important when external heat sink is attached on package top.



- Ψ_{JT} Junction to top thermal resistance:

  $\Psi_{JT} = (T_{J,MAX} - T_{TOP}) / P_H$
  Where T_{Top} is the temperature at the top center of the package



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