Qualcomm

Qualcomm Technologies, Inc.

QCC744 Thermal Analysis

Standard JEDEC Thermal Simulation Report

80-WL740-13 Rev. AB

March 3, 2025

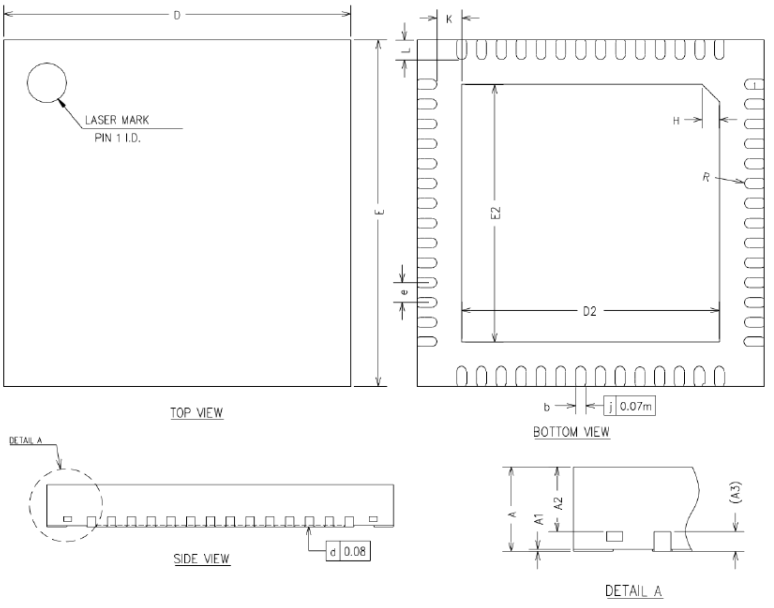
1 Introduction

This thermal simulation report is aimed to evaluate the thermal performance of QCC744. The software Icepak is utilized.

2 Simulation conditions

PCB type	Symbol	Definition	Unit
4 layers (2s2p)	$R_{\Theta JA}$	Thermal resistance, junction to ambient environment (natural convection)	°C/W
4 layers (2s2p)	$R_{\Theta JB}$	Thermal resistance, junction to board (forced convection)	°C/W
-	$R_{\Theta JC}$	Thermal resistance, junction to case (forced convection)	°C/W
4 layers (2s2p)	Ψ_{JT}	Thermal property parameter, junction to top thermal (forced convection)	°C/W

3 Package model



(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20REF	
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.10	5.20	5.30
E2	5.10	5.20	5.30
e	0.30	0.40	0.50
H		0.35REF	
K		0.50REF	
L	0.35	0.40	0.45
R	0.09	–	–

Figure 1 QCC744 QFN-56 package drawing

4 Material properties and structure parameters

Table 1 Thermal properties of component material

Component	Material	Size (mm x mm x mm)	Thermal conductivity (W/m.K)
EMC	G700Q-B	7 x 7 x 0.85	0.96
Die	Silicon	3.2993 x 3.2993 x 0.15/1.13 x 1.24 x 0.15	148
Frame	Cu	Import	386
DAF	HR-5104T-25	1.13 x 1.24 x 0.025	0.3
DAA	EN4900F	3.2993 x 3.2993 x 0.02	2.0

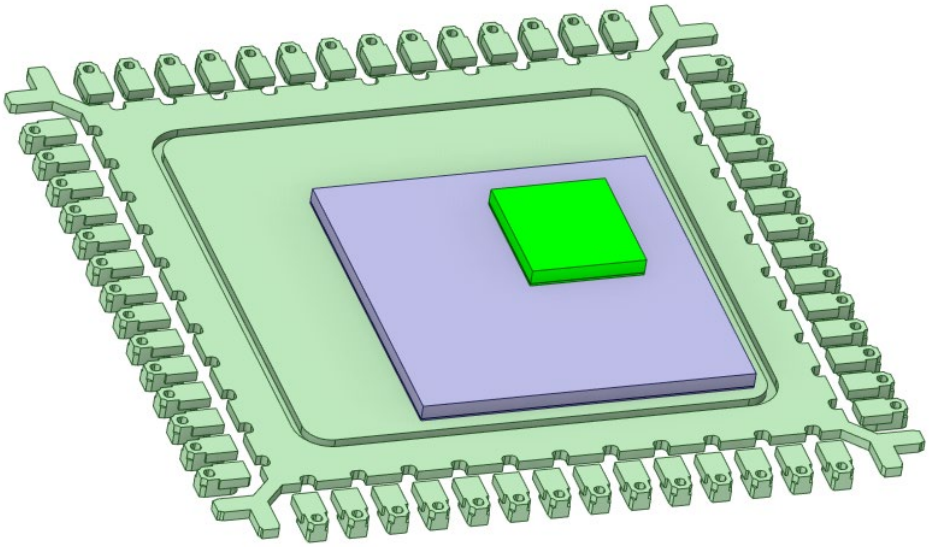


Figure 2 3D structure

Table 2 Thermal resistance data

Power	PCB type	Convection type	Ambient temperature	T_J (J_A) ℃	Θ_{JA} ℃/W	T_J (J_B) ℃	Θ_{JB} ℃/W	T_J (J_C) ℃	Θ_{JC} ℃/W
Die1:1W Die2:0.054W	2S2P	Natural convection	25℃	59.92	33.13	52.69	26.27	40.73	14.92

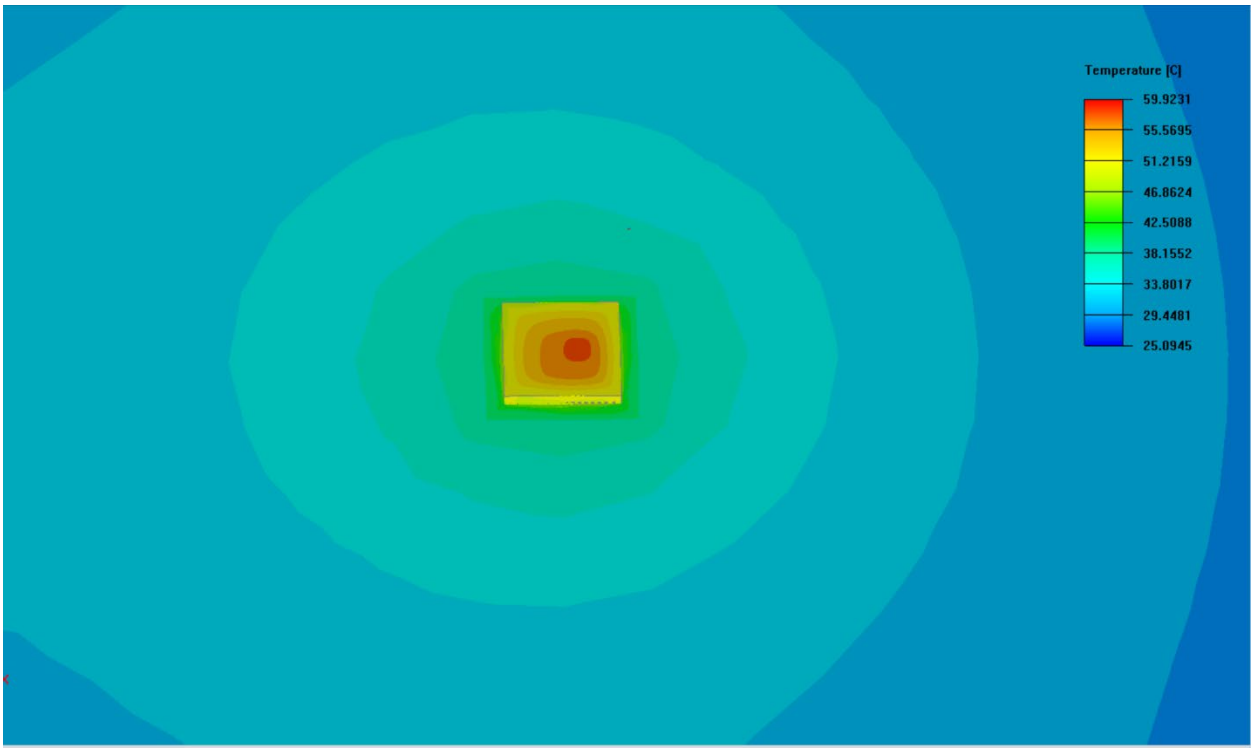


Figure 3 Thermal resistance of θ_{JA}

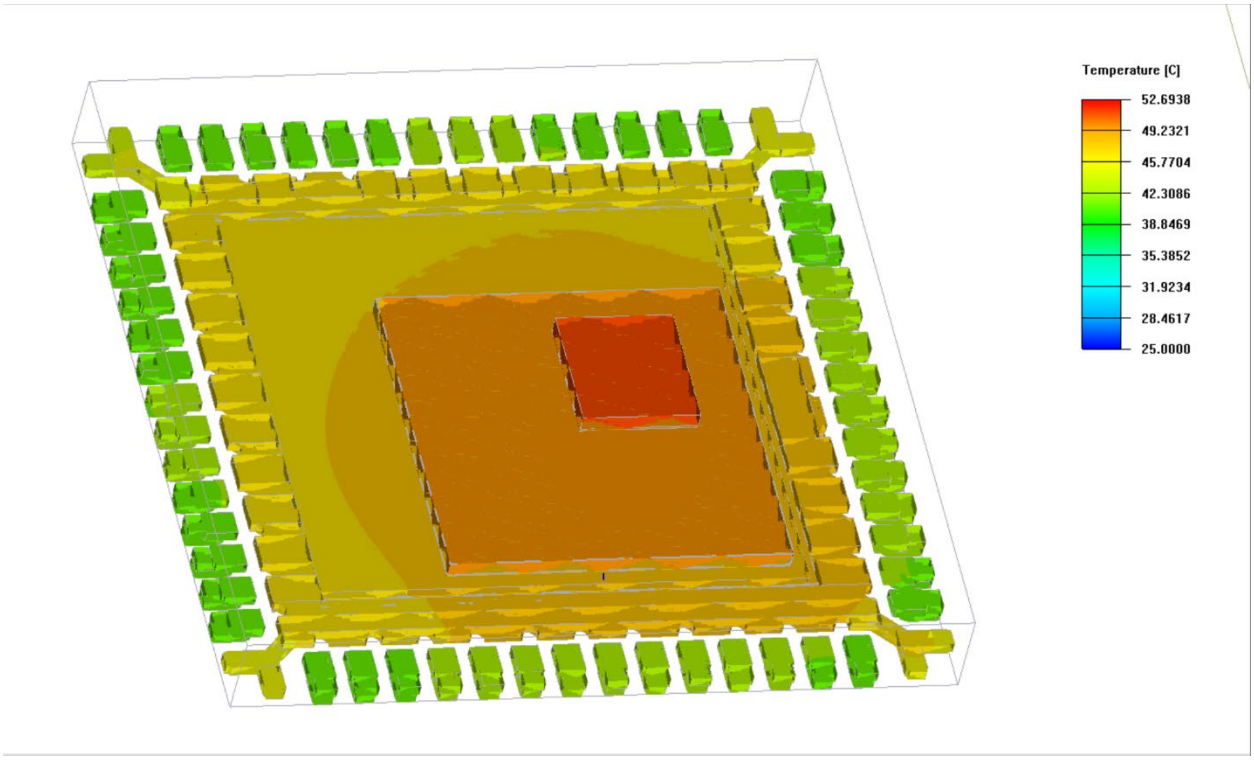


Figure 4 Thermal resistance of θ_{JB}

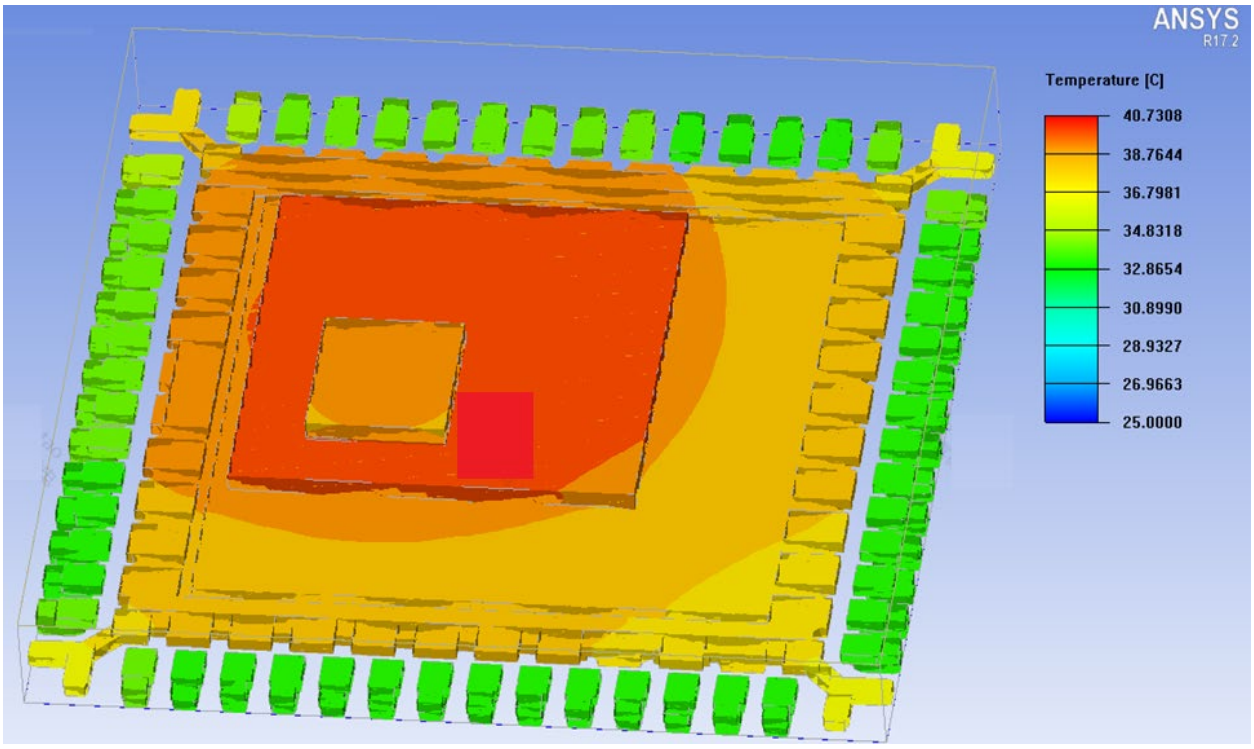


Figure 5 Thermal resistance of θ_{JC}

A Appendix

- θ_{JA} Junction to ambient thermal resistance:

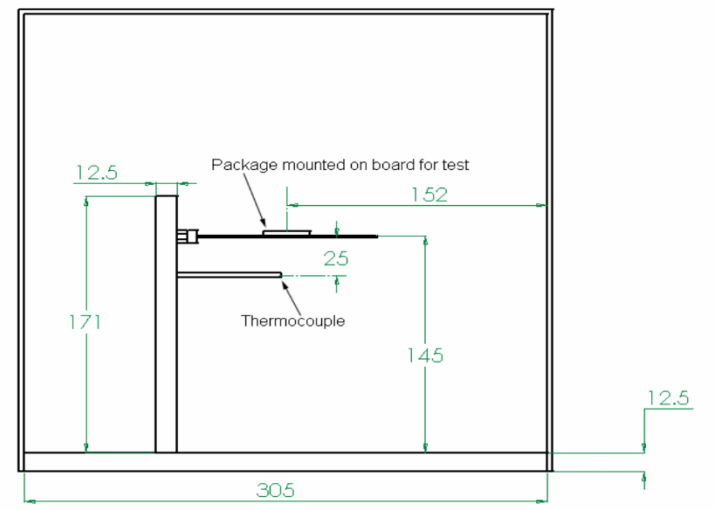
  $\theta_{JA} = (T_{J,\ MAX} - T_A)/P_H$

  Where $T_{J,\ MAX}$ = maximum junction temperature.

  T_A = ambient temperature

  P_H = total power dissipation

  θ_{JA} represents the resistance of the heat flows from the chip to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance.

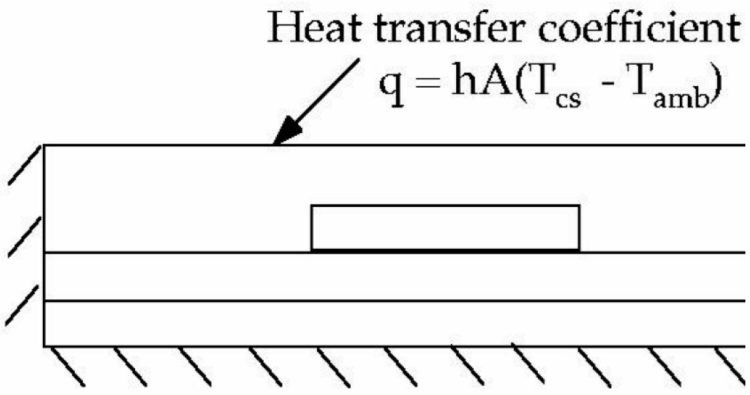


- θ_{JC} Junction to case thermal resistance:

  $\theta_{JC} = (T_{J,\ MAX} - T_C)/P_H$

  Where T_C = case temperature which is monitoring on package surface

  θ_{JC} represents the thermal resistance between the chip to package top case. θ_{JC} is important when external heat sink is attached on package top.



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