QCS6490 CSI IRQ STATUS Register Description

Application Note

80-xxxxx-x x

August 25, 2025

CSID IRQ status registers:

CSID_CSI2_RX_IRQ_STATUS Register

Bit	Name	Description
27	INFO_RST_DONE	Reset Strobe has finished resetting its target.
26	ERROR_TG_FIFO_OVERFLOW	Test generator output FIFOs overflowed. Fatal error, TG must be reset to recover.
25	INFO_TG_DONE	Test generator has completed its tasks.
24	ERROR_UNBOUNDED_FRAME	A Frame Start was not closed by a Frame End OR a Frame End does not have corresponding Frame Start.
23	ERROR_STREAM_UNDERFLOW	Fatal error, requires full csid reset. Received payload (for a long packet) has fewer bytes than specified in the packet header's word count.
22	ERROR_UNMAPPED_VC_DT	A long packet has a VC/DT combination not mapped to an IPP or RDI path. The header of the first error packet will be captured in CSID_CAPTURED_UNMAPPED_LONG_PKT_HDR .
21	ERROR_MMAPPED_VC_DT	A long packet has a VC/DT_ID combination mapped to more than one VC/DT combination.
20	ERROR_ECC	A short or long packet is corrupted and cannot be recovered.
19	ERROR_CRC	The calculated CRC of a long packet does not match the transmitted (expected) CRC.
18	ERROR_LANE3_FIFO_OVERFLOW	Fatal error, requires full csid reset. Input FIFO 3 overflowed. Possible causes: PHY clock is too fast relative to internal clock OR too much skew between data lanes.
17	ERROR_LANE2_FIFO_OVERFLOW	Fatal error, requires full csid reset. Input FIFO 2 overflowed. Possible causes: PHY clock is too fast relative to internal clock OR too much skew between data lanes.
16	ERROR_LANE1_FIFO_OVERFLOW	Fatal error, requires full csid reset. Input FIFO 1 overflowed. Possible causes: PHY clock is too fast relative to internal clock OR too much skew between data

		lanes.
15	ERROR_LANE0_FIFO_OVERFLOW	Fatal error, requires full csid reset. Input FIFO 0 overflowed. Possible causes: PHY clock is too fast relative to internal clock OR too much skew between data lanes.
14	WARNING_ECC	A short or long packet header with 1 bit of corruption is properly corrected.
13	ERROR_CPHY_PH_CRC	All CPHY packet headers received are corrupted and CRC mismatches are produced.
12	ERROR_CPHY_SOT_RECEPTION	One or more lanes received less than 2 SOTs.
11	ERROR_CPHY_EOT_RECEPTION	One or more lanes did not receive an EOT.
10	INFO_CPHY_PKT_HDR_CAPTURED	The first CPHY packet header matching the VC/DT specified in CPHY_PKT_CAPTURE_VC_DT has been captured. The captured header is in CSID_CAPTURED_CPHY_PKT_HDR.
9	INFO_SHORT_PKT_CAPTURED	The first short packet matching the VC/DT specified in SHORT_PKT_CAPTURE_VC has been captured. The packet is present in CAPTURED_SHORT_PKT.
8	INFO_LONG_PKT_CAPTURED	The first long packet header matching the VC/DT specified in LONG_PKT_CAPTURE_VC_DT has been captured. The header and footer are present in CSID_CAPTURED_LONG_PKT_HDR and CSID_CAPTURED_LONG_PKT_FTR, respectively.
7	INFO_PHY_DL3_SOT_CAPTURED	An SOT (Start of Transmission) on PHY Data Lane 3. (Unused when CPHY enabled.)
6	INFO_PHY_DL2_SOT_CAPTURED	An SOT (Start of Transmission) on PHY Data Lane 2.
5	INFO_PHY_DL1_SOT_CAPTURED	An SOT (Start of Transmission) on PHY Data Lane 1.
4	INFO_PHY_DL0_SOT_CAPTURED	An SOT (Start of Transmission) on PHY Data Lane 0.
3	INFO_PHY_DL3_EOT_CAPTURED	An EOT (End of Transmission) on PHY Data Lane 3. (Unused when CPHY enabled.)
2	INFO_PHY_DL2_EOT_CAPTURED	An EOT (End of Transmission) on PHY Data Lane 2.
1	INFO_PHY_DL1_EOT_CAPTURED	An EOT (End of Transmission) on PHY Data Lane 1.
0	INFO_PHY_DL0_EOT_CAPTURED	An EOT (End of Transmission) on PHY Data Lane 0.

CSID_CSI2_RDIN_IRQ_STATUS Register

Bit	Name	Description
15	CCIF_VIOLATION	The output CCIF has a violation with respect to frame timing.
14	ERROR_LINE_COUNT	The line count of the current frame does not match the previous frame's line count.
13	ERROR_PIX_COUNT	The pixel count of the current line does not match the previous line's pixel count.
12	INFO_INPUT_SOF	Start of frame occurred (pre frame drop).
11	INFO_INPUT_SOL	Start of line occurred (pre frame drop).
10	INFO_INPUT_EOL	End of line occurred (pre frame drop).
9	INFO_INPUT_EOF	End of frame occurred (pre frame drop).
8	INFO_FRAME_DROP_SOF	Start of frame occurred (post frame drop).
7	INFO_FRAME_DROP_SOL	Start of line occurred (post frame drop).
6	INFO_FRAME_DROP_EOL	End of line occurred (post frame drop).
5	INFO_FRAME_DROP_EOF	End of frame occurred (post frame drop).
4	INFO_SUBSAMPLED_SOF	Start of frame occurred (post frame drop and post IRQ sub-sample).
3	INFO_SUBSAMPLED_EOF	End of frame occurred (post frame drop and post IRQ sub-sample).
2	ERROR_FIFO_OVERFLOW	Output FIFO overflowed.
1	INFO_RST_DONE	Software reset is complete.
0	RESERVED	Reserved

CSID_CSI2_IPP_IRQ_STATUS Register

Bit	Name	Description
15	CCIF_VIOLATION	The output CCIF has a violation with respect to frame timing.
14	ERROR_LINE_COUNT	The line count of the current frame does not match the previous frame's line count.
13	ERROR_PIX_COUNT	The pixel count of the current line does not match the previous line's pixel count.
12	INFO_INPUT_SOF	Start of frame occurred (pre frame drop).
11	INFO_INPUT_SOL	Start of line occurred (pre frame drop).
10	INFO_INPUT_EOL	End of line occurred (pre frame drop).
9	INFO_INPUT_EOF	End of frame occurred (pre frame drop).
8	INFO_FRAME_DROP_SOF	Start of frame occurred (post frame drop).
7	INFO_FRAME_DROP_SOL	Start of line occurred (post frame drop).
6	INFO_FRAME_DROP_EOL	End of line occurred (post frame drop).
5	INFO_FRAME_DROP_EOF	End of frame occurred (post frame drop).
4	INFO_SUBSAMPLED_SOF	Start of frame occurred (post frame drop and post IRQ sub-sample).
3	INFO_SUBSAMPLED_EOF	End of frame occurred (post frame drop and post IRQ sub-sample).
2	ERROR_FIFO_OVERFLOW	Output FIFO overflowed.
1	INFO_RST_DONE	Software reset is complete.
0	RESERVED	Reserved.

CSI PHY IRQ status registers:

CSI_COMMON_STATUS0 | Offset=0xb0

Bit	Name	Description
7 : 7	CSI_COMMON_STATUS0_7	IRQ_LN0_ULPM_EXIT Lane 0 ULPM exit IRQ indicates exit from ULPM mode
6 : 6	CSI_COMMON_STATUS0_6	IRQ_LN0_ULPM_ENTRY Lane 0 ULPM entry IRQ indicates entry into ULPM mode
5 :	CSI_COMMON_STATUS0_5	IRQ_LN0_ULPM_ERR Lane 0 ULPM error IRQ indicates an illegal state happens between ULPM entry and exit
4 :	CSI_COMMON_STATUS0_4	IRQ_LN0_ERR_SOT_SYNC Lane 0 SOT error detected IRQ indicates that received SOT is corrupted
3 :	CSI_COMMON_STATUS0_3	IRQ_LN0_ERR_SOT Lane 0 SOT one bit error correction IRQ indicates that received SOT may have 1-bit error when this feature is enabled
2 :	CSI_COMMON_STATUS0_2	IRQ_LN0_CTL_ERR Lane 0 control error IRQ indicates illegal LP state transition such as LP01 not followed by LP00
1 :	CSI_COMMON_STATUS0_1	IRQ_LN0_CMD_ERR Lane 0 command error IRQ

Bit	Name	Description
		indicates an error in ESCAPE mode entry command
0 :	CSI_COMMON_STATUS0_0	IRQ_LN0_FIFO_OFLOW Lane 0 FIFO over flow IRQ indicates RX FIFO overflow which may be caused by wrong CSI clock frequency

CSI_COMMON_STATUS1 | Offset=0xb4

Bit	Name	Description
7 :	CSI_COMMON_STATUS1_7	IRQ_LN1_HS_ENTRY_ERROR Lane High Speed entry error IRQ IRQ indicates illegal LP state during HS entry
6 :	CSI_COMMON_STATUS1_6	IRQ_LN1_HS_EXIT_ERROR Lane 1 High Speed exit error IRQ IRQ indicates illegal LP state during HS exit
5 :	CSI_COMMON_STATUS1_5	IRQ_LN1_ESCAPE_ENTRY_ERROR Lane 1 ESCAPE entry error IRQ IRQ indicates an error during ESCAPE mode entry
4 :	CSI_COMMON_STATUS1_4	IRQ_LN1_ESCAPE_COMMAND_ERROR Lane 1 ESCAPE command error IRQ IRQ indicates error in ESCAPE mode command
3 :	CSI_COMMON_STATUS1_3	IRQ_LN1_ESCAPE_EXIT_ERROR Lane 1 ESCAPE exit IRQ IRQ indicates an error during ESCAPE mode exit
2 :	CSI_COMMON_STATUS1_2	IRQ_LN1_PDQ_SYNC Lane 1 PDQ SYNC IRQ IRQ indicates that PDQ SYNC was detected
1 :	CSI_COMMON_STATUS1_1	IRQ_LN1_FIFO_OFLOW Lane 1 FIFO overflow IRQ IRQ

Bit	Name	Description
		indicates RX FIFO overflow which may be caused by wrong CSI clock frequency
0 :	CSI_COMMON_STATUS1_0	IRQ_LN0_RXSYNC Lane 0 SOT detected IRQ indicates received SOT is valid

CSI_COMMON_STATUS2 | Offset=0xb8

Bit	Name	Description
7 :	CSI_COMMON_STATUS2_7	IRQ_LN2_CTL_ERR Lane 2 control error IRQ IRQ indicates illegal LP state transition such as LP01 not followed by LP00
6 :	CSI_COMMON_STATUS2_6	IRQ_LN2_CMD_ERR Lane 2 command error IRQ IRQ indicates an error in ESCAPE mode entry command
5 :	CSI_COMMON_STATUS2_5	IRQ_LN2_FIFO_OFLOW Lane 2 FIFO over flow IRQ IRQ indicates RX FIFO overflow which may be caused by wrong CSI clock frequency
4 :	CSI_COMMON_STATUS2_4	IRQ_LN1_FIRST_SYNC_FLAG Lane 1 first SYNC pattern IRQ IRQ indicates first SYNC pattern was detected
3 :	CSI_COMMON_STATUS2_3	IRQ_LN1_SECOND_SYNC_FLAG Lane 1 second SYNC pattern IRQ IRQ indicates second SYNC pattern was detetced

Bit	Name	Description
2 :	CSI_COMMON_STATUS2_2	IRQ_LN1_DEMAPPING_ERROR Lane 1 demapping error IRQ IRQ indicates an error in demapping function
1 :	CSI_COMMON_STATUS2_1	IRQ_LN1_ULPS_ENTRY Lane ULPS mode entry IRQ IRQ indicates entry into ULPS mode
0 :	CSI_COMMON_STATUS2_0	IRQ_LN1_MISSING_POST Lane 1 missing POST IRQ IRQ indicates post was not detected; this may be caused by a short POST period

CSI_COMMON_STATUS3 | Offset=0xbc

Bit	Name	Description
7 :	CSI_COMMON_STATUS3_7	IRQ_LN3_PDQ_SYNC Lane 3 PDQ SYNC IRQ IRQ indicates that PDQ SYNC was detected
6 :	CSI_COMMON_STATUS3_6	IRQ_LN3_FIFO_OFLOW Lane 3 FIFO overflow IRQ IRQ indicates RX FIFO overflow which may be caused by wrong CSI clock frequency
5 :	CSI_COMMON_STATUS3_5	IRQ_LN2_RXSYNC Lane 2 SOT detected IRQ IRQ indicates received SOT is valid
4 :	CSI_COMMON_STATUS3_4	IRQ_LN2_ULPM_EXIT Lane 2 ULPM exit IRQ IRQ indicates exit from ULPM mode
3 :	CSI_COMMON_STATUS3_3	IRQ_LN2_ULPM_ENTRY Lane 2 ULPM entry IRQ IRQ indicates entry into ULPM mode

Bit	Name	Description
2 :	CSI_COMMON_STATUS3_2	IRQ_LN2_ULPM_ERR Lane 2 ULPM error IRQ IRQ indicates an illegal state happens between ULPM entry and exit
1 :	CSI_COMMON_STATUS3_1	IRQ_LN2_ERR_SOT_SYNC Lane 2 SOT error detection IRQ IRQ indicates that received SOT is corrupted
0 :	CSI_COMMON_STATUS3_0	IRQ_LN2_ERR_SOT Lane 2 SOT error correction IRQ IRQ indicates that received SOT may have 1-bit error when this feature is enabled

CSI_COMMON_STATUS4 | Offset=0xc0

Bit	Name	Description
7 :	CSI_COMMON_STATUS4_7	IRQ_LN3_DEMAPPING_ERROR Lane 3 demapping error IRQ IRQ indicates an error in demapping function
6 :	CSI_COMMON_STATUS4_6	IRQ_LN3_ULPS_ENTRY Lane 3 ULPS entry IRQ IRQ indicates entry into ULPS mode
5 :	CSI_COMMON_STATUS4_5	IRQ_LN3_MISSING_POST Lane 3 missing POST IRQ IRQ indicates post was not detected; this may be caused by a short POST period
4 :	CSI_COMMON_STATUS4_4	IRQ_LN3_HS_ENTRY_ERROR Lane 3 High Speed entry error IRQ IRQ indicates illegal LP state during HS entry
3 :	CSI_COMMON_STATUS4_3	IRQ_LN3_HS_EXIT_ERROR Lane 3 High Speed exit error IRQ IRQ indicates illegal LP state during HS exit

Bit	Name	Description
2 :	CSI_COMMON_STATUS4_2	IRQ_LN3_ESCAPE_ENTRY_ERROR Lane 3 ESCAPE entry error IRQ IRQ indicates an error during ESCAPE mode entry
1 :	CSI_COMMON_STATUS4_1	IRQ_LN3_ESCAPE_COMMAND_ERROR Lane 3 ESCAPE command error IRQ IRQ indicates error in ESCAPE mode command
0 :	CSI_COMMON_STATUS4_0	IRQ_LN3_ESCAPE_EXIT_ERROR Lane 3 ESCAPE exit error IRQ

CSI_COMMON_STATUS5 | Offset=0xc4

Bit	Name	Description
7 :	CSI_COMMON_STATUS5_7	IRQ_LN4_ULPM_EXIT Lane 4 ULPM exit IRQ IRQ indicates exit from ULPM mode
6 :	CSI_COMMON_STATUS5_6	IRQ_LN4_ERR_SOT_SYNC Lane 4 SOT error detected IRQ IRQ indicates that received SOT is corrupted
5 :	CSI_COMMON_STATUS5_5	IRQ_LN5_PDQ_SYNC Lane 5 PDQ SYNC IRQ IRQ indicates that PDQ SYNC was detected
4 :	CSI_COMMON_STATUS5_4	IRQ_LN4_CTL_ERR Lane 4 control error IRQ IRQ indicates illegal LP state transition such as LP01 not followed by LP00
3 :	CSI_COMMON_STATUS5_3	IRQ_LN4_CMD_ERR Lane 4 command error IRQ IRQ indicates an error in ESCAPE mode entry command

Bit	Name	Description
2 :	CSI_COMMON_STATUS5_2	IRQ_LN4_FIFO_OFLOW Lane 4 FIFO overflow IRQ IRQ indicates RX FIFO overflow which may be caused by wrong CSI clock frequency
1 :	CSI_COMMON_STATUS5_1	IRQ_LN3_FIRST_SYNC_FLAG Lane 3 first SYNC pattern IRQ IRQ indicates first SYNC pattern was detected
0 :	CSI_COMMON_STATUS5_0	IRQ_LN3_SECOND_SYNC_FLAG Lane 3 second SYNC pattern IRQ IRQ indicates second SYNC pattern was detetced

CSI_COMMON_STATUS6 | Offset=0xc8

Bit	Name	Description
7 :	CSI_COMMON_STATUS6_7	IRQ_LN5_ESCAPE_ENTRY_ERROR Lane 5 ESCAPE entry error IRQ IRQ indicates an error during ESCAPE mode entry
6 :	CSI_COMMON_STATUS6_6	IRQ_LN5_ESCAPE_COMMAND_ERROR Lane 5 ESCAPE command error IRQ IRQ indicates an error in ESCAPE mode entry command
5 :	CSI_COMMON_STATUS6_5	IRQ_LN5_ESCAPE_EXIT_ERROR Lane 5 ESCAPE exit error IRQ IRQ indicates an error during ESCAPE mode exit
4 :	CSI_COMMON_STATUS6_4	IRQ_LN5_SYNC_BIT_ERROR Lane 5 SYNC one bit error IRQ IRQ indicates that received SOT may have 1-bit error when this feature is enabled

Bit	Name	Description
3 :	CSI_COMMON_STATUS6_3	IRQ_LN5_FIFO_OFLOW Lane 5 FIFO overflow IRQ IRQ indicates RX FIFO overflow which may be caused by wrong CSI clock frequency
2 :	CSI_COMMON_STATUS6_2	IRQ_LN4_RXSYNC Lane 4 SOT detected IRQ IRQ indicates received SOT is valid
1 :	CSI_COMMON_STATUS6_1	IRQ_LN4_ULPM_ENTRY Lane 4 ULPM entry IRQ IRQ indicates entry into ULPM mode
0 :	CSI_COMMON_STATUS6_0	IRQ_LN4_ULPM_ERR Lane 4 ULPM error IRQ IRQ indicates an illegal state happens between ULPM entry and exit

CSI_COMMON_STATUS7 | Offset=0xcc

Bit	Name	Description
7 :	CSI_COMMON_STATUS7_7	IRQ_LN6_FIFO_OFLOW Lane 6 FIFO overflow IRQ IRQ indicates RX FIFO overflow which may be caused by wrong CSI clock frequency
6 :	CSI_COMMON_STATUS7_6	IRQ_LN5_FIRST_SYNC_FLAG Lane 5 first SYNC pattern IRQ IRQ indicates first SYNC pattern was detected
5 :	CSI_COMMON_STATUS7_5	IRQ_LN5_SECOND_SYNC_FLAG Lane 5 second SYNC pattern IRQ IRQ indicates second SYNC pattern was detetced
4 :	CSI_COMMON_STATUS7_4	IRQ_LN5_DEMAPPING_ERROR Lane 5 demapping error IRQ IRQ indicates an error in demapping

Bit	Name	Description
		function
3 :	CSI_COMMON_STATUS7_3	IRQ_LN5_ULPS_ENTRY Lane 5 ULPS entry IRQ IRQ indicates entry into ULPS mode
2 :	CSI_COMMON_STATUS7_2	IRQ_LN5_MISSING_POST Lane 5 missing POST IRQ IRQ indicates post was not detected; this may be caused by a short POST period
1 :	CSI_COMMON_STATUS7_1	IRQ_LN5_HS_ENTRY_ERROR Lane 5 High Speed entry error IRQ IRQ indicates illegal LP state during HS entry
0 :	CSI_COMMON_STATUS7_0	IRQ_LN5_HS_EXIT_ERROR Lane 5 High Speed exit error IRQ IRQ indicates illegal LP state during HS exit

CSI_COMMON_STATUS8 | Offset=0xd0

Bit	Name	Description
7 :	CSI_COMMON_STATUS8_7	IRQ_LN6_RXSYNC Lane 6 SOT detected IRQ IRQ indicates received SOT is valid
6 :	CSI_COMMON_STATUS8_6	IRQ_LN6_ULPM_EXIT Lane 6 ULPM exit IRQ IRQ indicates exit from ULPM mode
5 :	CSI_COMMON_STATUS8_5	IRQ_LN6_ULPM_ENTRY Lane 6 ULPM entry IRQ IRQ indicates entry into ULPM mode
4 :	CSI_COMMON_STATUS8_4	IRQ_LN6_ULPM_ERR Lane 6 ULPM error IRQ IRQ indicates an illegal state happens between ULPM entry and exit

Bit	Name	Description
3 :	CSI_COMMON_STATUS8_3	IRQ_LN6_ERR_SOT_SYNC Lane 6 SOT error detected IRQ IRQ indicates that received SOT is corrupted
2 :	CSI_COMMON_STATUS8_2	IRQ_LN6_ERR_SOT Lane 6 SOT one bit error correction IRQ IRQ indicates that received SOT may have 1-bit error when this feature is enabled
1 :	CSI_COMMON_STATUS8_1	IRQ_LN6_CTL_ERR Lane 6 control error IRQ IRQ indicates illegal LP state transition such as LP01 not followed by LP00
0 :	CSI_COMMON_STATUS8_0	IRQ_LN6_CMD_ERR Lane 6 command error IRQ IRQ indicates an error in ESCAPE mode entry command

CSI_COMMON_STATUS9 | Offset=0xd4

Bit	Name	Description
7 :	CSI_COMMON_STATUS9_7	IRQ_LNCK_CLK_STOP IRQ indicates LNCK clock stop
6 :	CSI_COMMON_STATUS9_6	IRQ_LNCK_CLK_START IRQ indicates LNCK clock start
5 :	CSI_COMMON_STATUS9_5	IRQ_LN6_CLK_STOP IRQ indicates LN6 clock stop when used as clock lane
4 :	CSI_COMMON_STATUS9_4	IRQ_LN6_CLK_START IRQ indicates LN6 clock start when used as clock lane
3 :	CSI_COMMON_STATUS9_3	IRQ_LN6_CAL_DONE IRQ indicates lane 6 calibration was completed

Bit	Name	Description
2 :	CSI_COMMON_STATUS9_2	IRQ_LN4_CAL_DONE IRQ inidicates lane 4 calibration was completed
1 :	CSI_COMMON_STATUS9_1	IRQ_LN2_CAL_DONE IRQ indicates lane 2 calibration was completed
0 :	CSI_COMMON_STATUS9_0	IRQ_LN0_CAL_DONE IRQ indicates lane 0 calibration was completed

CSI_COMMON_STATUS10 | Offset=0xd8

Bit	Name	Description
7 :	CSI_COMMON_STATUS10_7	IRQ_LNCK_ULPM_EXIT Lane CKULPM exit
6 :	CSI_COMMON_STATUS10_6	IRQ_LNCK_ULPM_ENTRY Lane CK ULPM entry
5 :	CSI_COMMON_STATUS10_5	IRQ_LNCK_ULPM_ERR Lane CK ULPM error
4 :	CSI_COMMON_STATUS10_4	IRQ_LNCK_ERR_SOT_SYNC Lane CK SYNC error correction
3 :	CSI_COMMON_STATUS10_3	IRQ_LNCK_ERR_SOT Lane CK SYNC error detection
2 :	CSI_COMMON_STATUS10_2	IRQ_LNCK_CTL_ERR Lane CK control error
1 :	CSI_COMMON_STATUS10_1	IRQ_LNCK_CMD_ERR Lane CK command error
0 :	CSI_COMMON_STATUS10_0	IRQ_LNCK_FIFO_OFLOW (Not supported)